Abstract

Video compression enables transmission and storage of enormous amount of video data. In spite of rapid progress in storage and transmission media, video compression remains an important constituent of video codec. Video data consists of a time sequence of image frames, and there exists a huge amount of redundancy in temporal domain. Video compression can be realized by removing the temporal redundancies in an efficient way. Motion Estimation (ME), which tries to remove the temporal redundancies, is the principal component of a video encoding system. Of all the components of a video encoder, the ME module consumes the lions share of power. A very simple arithmetic computation is required for ME. However, frequent memory access associated with ME affects the overall speed of operation and the power consumption. The present work has therefore focused on design and development of several fast ME architectures characterized by high processing speed, low power, and low area making them suitable for portable video application devices that are typically operated by battery power and involve real time operation. Following results have emerged in the process. A high performance architecture has been developed for the Unrestricted Center Biased Diamond Search (UCBDS) algorithm that is used in videoconferencing applications. An intelligent data arrangement has been used in this design to reduce the power consumption and to achieve a high speed of operation. Efficient architectures for sub-pixel ME have also been developed. The architectures presented for half-pixel and quarter-pixel ME have been optimized in order to get a high speed of operation and low power

consumption. Moreover, the present work has conceived fast ME by combining One Bit Transformation (1BT) for fixed block size and single reference frame. Fast 1BT based ME architectures for variable block size and single reference frame and multiple reference frames have also been developed. The scope of the present work also includes fast ME algorithms based on the pixel truncation. An appropriate architecture has also been developed for implementing the proposed ME algorithm. In the present work, all the proposed architectures have been synthesized and analyzed for power and maximum operating frequencies in FPGA as well as ASIC platforms.

Keywords: block matching motion estimation algorithms, fast search motion estimation architecture, sub-pixel motion estimation, one-bit transformation, variable block size motion estimation, pixel truncation.