Abstract

Digital video is becoming ubiquitous and its seamless transmission via wired and wireless media calls for increased compression efficiency of video encoders. Motion estimation and motion compensation play important roles in achieving high compression by reducing the spatial and temporal redundancy inherent in the video sequences. Although Full Search Block Matching Algorithm (FSBMA) gives the best possible reconstructed video, it has high computational complexity and requires a high bit rate for broadcasting real time videos at low distortion. The present work has, therefore, focused on algorithms which gives rise to the best possible reconstructed video at low bit rate and its less complex VLSI implementation.

In the first part of the thesis, the performance of different suboptimal fast Block Matching Algorithms (BMAs) have been compared in terms of average Peak Signal-to-Noise Ratio (PSNR) of the reconstructed video frames, Average Number of Search Points (ANSP) for generating a Motion Vector (MV) and the required hardware complexity. Overall, the Adaptive Rood Pattern Search (ARPS) Algorithm gives rise to better result while considering PSNR and ANSP together and is suitable for less complex hardware realization. Hence, the ARPS algorithm has been adopted for motion estimation in this work. The corresponding results are highlighted therein.

While BMAs are simple, they tacitly assume that motion in the video frame is purely translational which, is not always true. BMA cannot model non-translational motion like rotation, shear and zoom. It may also cause blocking artifacts. These disadvantages can be overcome by using Mesh Based Motion Estimation (MBME), which employs non-translational motion models like Affine Transformation at the expense of increased computational complexity. Moreover, the MBME generates a continuously varying motion field. Triangular mesh is commonly used and it is modelled by Affine Transformation. Hence a Fixed Mesh Based ARPS (FMBARPS) Algorithm has been proposed for deformable motion estimation using right-angled triangular patches.

Although the FMBARPS Algorithm has addressed almost all limitations of BMAs, it suffers from the inability to adapt to the changing motion contents in a video frame. While smaller sized polygons that constitute the mesh of the MBME technique can model almost all motion contents of a fast motion video frame, it is likely to cause unnecessary increase in computations for slow motion video. This points to the need of a hierarchical mesh based motion estimation termed as Hierarchical Mesh Based ARPS (HMBARPS) Algorithm in which, the motion estimation process begins with a larger polygonal patch, and the polygons get recursively subdivided into smaller ones when the MV associated with any one of the nodes exceeds a threshold value. This has led us to develop an architecture for HMBARPS algorithm.

The effectiveness of the proposed algorithms and corresponding architectures reported in this thesis has been illustrated and compared with recently reported results. It has been observed that the proposed techniques have brought forth performance that is decidedly better than the existing results.

Key words: Video Compression, Block Matching Algorithms (BMAs), Adaptive Rood Pattern Search (ARPS) Algorithm, Deformable Mesh based Motion Estimation, VLSI Design.