Thesis Title: ADAPTIVE BUS-ENCODING FOR TRANSITION REDUCTION ON OFF-CHIP AND ON-CHIP BUSES

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ABSTRACT

The dissertation presents adaptive encoding techniques for the reduction of self-transition activity in high capacitance off-chip buses since power dissipation associated with those buses can be significant for high speed communication and coupling-transition activity reduction in on-chip buses as power dissipation in on-chip buses is mostly dominated by coupling between bit lines. Both proposed adaptive techniques rely on the observation of data characteristics over fixed window sizes. In every observation window proposed off-chip method forms a cluster or sub-group of bit-lines having highly correlated switching patterns. It uses XOR operation to reduce the transitional correlation among them which finally leads to self-transitions reduction. The proposed on-chip encoding exploits coupling correlation among adjacent bit-lines in each observation window and selectively encodes a group or cluster of bit lines by means of XOR operation which reduces coupling transitions. The proposed off-chip and on-chip encoding methods utilize redundancy in space and time to prevent loss of information while retrieving data at the decoder. Analytical and experimental results demonstrate the self and coupling activity reduction by our adaptive encoding schemes outperform other existing encoding techniques for various data sets especially when data characteristics changes over time. We improve the overhead due to encoder and decoder by optimizing algorithm and hardware for proposed off-chip encoding, whereas for proposed on-chip encoding method we focus on computational complexity reduction at the algorithmic level only.

Keywords: Off-chip bus, On-chip bus, Bus encoding schemes, Bus Power reduction, Low power VLSI design, Interconnect power