Abstract

Dynamic Voltage Scaling (DVS) remains essential for saving dynamic power, yet to meet real-time deadlines in various emerging applications, such as embedded processors, internet-of-things, wireless sensor networks, smartphones, and a variety of portable devices. In Complementary Metal Oxide Semiconductor (CMOS) processors, a reduction in clock frequency reduces the power consumption; however, the energy consumption per clock cycle remains the same. Hence, the supply voltage is also lowered for further power and energy savings. A linear reduction in the supply voltage leads to a quadratic reduction in the energy consumption; thus, a DVS technique can be used to meet the performance/efficiency trade-off by dynamically varying the supply voltage. In an embedded system, a task scheduler provides optimized voltage levels for given tasks along with their deadlines, and a DC-DC converter is used to generate the required voltage levels from the available battery (supply) voltage. A DVS scheme further drastically improves the energy efficiency of a Power Amplifier (PA) by dynamically varying its supply voltage close to its envelope without violating the linearity.

This thesis primarily considers identifying suitable DC-DC converter topologies and developing high dynamic performance control techniques for reference tracking applications. A Digital Current Mode Control (DCMC) tuning method is developed in a synchronous buck converter to achieve near time-optimal recovery for step changes in load current and reference voltage. Thereafter, conflicting power circuit design criteria in existing DVS power supplies are identified. A Single-Inductor Multi-Output Level (SIMOL) buck converter is developed to overcome these problems. This topology is also extended to per-core DVS-enabled multi-core processors for fast transient recovery, reduced time and energy overheads, and improved energy efficiency. Finally, a high-performance Mixed-Signal Hysteretic Current Control (MSHCC) is developed for Envelope Tracking (ET) applications, and a new multi-capacitor architecture is proposed for tracking high-peak-to-average power signals. All the proposed DC-DC converters and control methods are experimentally verified.

Keywords: DC-DC converters, dynamic voltage scaling, envelope tracking, current mode control, buck converter, time-optimal recovery, multi-core processors, hysteretic control.