Abstract

Network-on-Chip (NoC) has emerged as a potential scalable interconnect solution to the ever-increasing inter-processor communication requirement in Multi-Processor Systems-on-Chip (MPSoCs). NoCs can significantly improve chip performance compared to the on-chip buses. However, only performance-aware NoC design may result in unacceptably high chip temperature. This reduces the reliability of the chip and may lead to drastic degradation in the system performance again. Moreover, chances of creating thermal hotspots increase as we further scale down the technology. This thesis concentrates on implementation of different thermal management techniques in high-level designs in NoC-based MPSoCs. It considers both Regular Mesh-based NoCs (RMNoCs) and Application-Specific NoCs (ASNoCs). A combined Particle Swarm Optimization and Simulated Annealing-based thermal-aware core and primary router placement technique has been developed for ASNoCs. It consists of three steps. Firstly, an area-optimized floorplanning of the cores has been conducted. Considering an overhead on that minimum area, a performance-aware floorplan has been generated next. Finally, a thermal-aware white space allocation and redistribution has been carried out on this performance-aware floorplan. After placing the cores and primary routers, a Discrete Particle Swarm Optimization based power-aware path synthesis has been carried out, which finds the positions of the links in the ASNoC floorplan. This technique also places junction- and secondary-routers in such a way that the total network power consumption and hence the chip temperature is minimized. The thesis also explores thermal management techniques in RMNoCs. A Simulated Annealing based thermal-aware Task Allocation and Scheduling method has been proposed, which jointly optimizes the task-to-core allocation and scheduling problems for periodic real-time applications. It is a platform-based procedure and is applicable for two- and three-dimensional (2D and 3D) RMNoCs containing both homogeneous and heterogeneous cores. Due to the increased distance of Si-layers from the heat sink, thermal management in 3D-RMNoCs becomes more crucial. Moreover, routers present in the topmost Si-layer often generate thermal hotspots due to their higher power density compared to the cores. To compensate this uneven temperature distribution in 3D-RMNoCs a Mixed Integer Linear Programming based routing technique has been proposed, which judiciously detours some of the traffic flows through the lower Si-layer.