ABSTRACT

A theoretical investigation has been carried out in order to optimize the Josephson junction parameters as well as its characteristics essential for realizing high-speed switching elements. An attempt has been made to show the impact of new high-Tc superconductors in Josephson electronics. A new definition of turn-on delay of a Josephson junction and its corresponding analytical model are suggested in order to remove the drawbacks and confusions existing in earlier investigations. Studies have been made for both low-Tc and high-Tc superconducting microstrip lines. A thorough investigation is conducted to obtain the optimized SQUID parameters and properties which are required for logic and memory circuits. The SQUID OR gate, AND gate amd memory cell have been designed using the optimized techniques. The dynamic response of these logic and memory circuits have been obtained. A thorough investigation is also made on the switching dynamics of resistive logic gates. Our concept of turn-on delay has been used to critically ascertain the switching speed of resistive logic gates. A new Cache memory cell using the Direct Coupled Isolation logic has been proposed. This is expected to be superior to the Cache memory cell suggested by IBM.

Key Words :

Superconductivity

Josephson junction

Superconducting stripline

Josephson logics

Josephson memories