Abstract

Over the past couple of decade, usage of diagnostic ultrasonography (USG) has got its precedence over other medical imaging modalities because of its non-invasive, ionizing-hazard-free and high resolution real-time imaging capabilities. But, a large number of world population cannot afford costlier and sophisticated medical facilities, as on an average 30% of the total world population are from the low income group. To address this problem this dissertation is targeted for the development of a real-time, low power, embedded solution for JPEG 2000 image compression based Back-end that can be a part of the portable USG system to increase its diagnostic capabilities and features without affecting the cost. Keeping these issues in mind, a novel depth invariant real time impulse noise removal algorithm (DIINoR) alongwith Discrete Wavelet Transform (DWT), Quantization and Tier-2 coder for JPEG 2000 image compression system are developed and implemented in FPGA. The proposed DIINoR algorithm can efficiently clean both the variable sized RAW images and fixed sized Back-end images. The DIINoR algorithm is then implemented both in MATLAB and in Xilinx platform on Virtex5 XC5VLX330T device and it runs at a maximum clock frequency of 249.48 MHz. As a part of implementing the JPEG 2000 image compression system, a high precision low-area unified architecture for lossy and lossless 2-D and 3-D multi-level DWT algorithm with a 20-bit precision and throughput of 2 results/cycle is proposed and implemented in FPGA, which gives the scope to extend the same Back-end design to JPEG 2000 Part 10 implementation. The design runs at a maximum clock frequency 245 MHz in Virtex5 XC5VLX330T device. A unique FPGA implementation of Tier-2 module comprising of main header, tile header and packet header for the JPEG 2000 image compression standard is done on Virtex5-XC5VLX330T device, which runs at a maximum clock frequency of 448 MHz. Finally, the datapath design for the Back-end of the USG system has been proposed in the dissertation. It shows that all the modules and the controller can be housed inside a single XC5VLX330T -2 FFG1738 FPGA to achieve an embedded real-time solution for the proposed Back-end.