# Abstract

In recent years, power dissipation has emerged as the key issue for the design of both high performance as well as battery operated hand-held portable systems. The advancement of VLSI technology has led to the emergence of high performance computing devices with multi-million transistors on the chip. These devices dissipate high power and require expensive arrangement for packaging and cooling to dissipate the heat generated inside the chip. Devices, which dissipate high power, are prone to a greater failure rate due to various heat related effects. Further, for battery operated systems, demand for longer battery charging cycle time is forcing designers for low power design. In recent years, the need for low power systems has caused a major paradigm shift in the synthesis of VLSI circuits.

Low power VLSI design can be achieved at various levels of the design abstraction from system and architecture levels down to logic and layout levels. Out of all these levels, however, low power design consideration at the logic level has potential advantages compared to the other levels. We, therefore, focus our investigation on low power circuit synthesis at the logic level only.

We have addressed six different problems related to the synthesis of low power high performance VLSI circuits at the logic level. Three prime logic styles, namely static CMOS, dynamic CMOS and pass-transistor logic have been chosen to study their effectiveness in the realization of low power high performance circuits. We have proposed techniques for the synthesis of delay-constrained dual-$V_T$ static CMOS circuits and energy-constrained dual-$V_T$ static CMOS circuits. The first approach is suitable for the synthesis of static CMOS circuits that provide the highest performance. The second approach is suitable for realizing circuits that require near minimum energy and cater to the need of battery operated portable systems, where battery life is of primary concern and the power-delay product is required to be minimized.

A novel logic design approach for the synthesis of dynamic CMOS circuits has been proposed. As domino/nora logic styles can implement only non-inverting logic, we have overcome this problem by using a novel concept called *unate decomposition.* With this decomposition, dynamic CMOS circuits using both the domino and nora logic are possible. Further, we have applied dual-$V_T$ technique in dynamic CMOS circuits to reduce leakage power dissipations. Dynamic CMOS circuits based on our approach are found to be superior in terms of area, delay, and power dissipations compared to their static CMOS counterparts and are believed to be a better choice for synthesizing low power high performance VLSI circuits.

Our approach of synthesizing PTL circuits is based on reduced unordered BDD (RUBDD), unlike the existing approaches, which are based on reduced ordered BDD (ROBDD). A ratio parameters based heuristic has been proposed to obtain RUBDD. It is found that the sizes of the BDDs based on our approach are smaller compared to those of the existing works. We have proposed technology mapping using LEAP-like cells, which makes technology mapping step simpler and gives the approach the same elegance as the standard cell-based synthesis. The dual-$V_T$ technique is also studied to reduce leakage power dissipation in PTL circuits. Like dynamic CMOS circuits, PTL circuits can also be considered as a viable alternative to static CMOS circuits, for both low power and high performance applications.

To calculate delay, switching power, and leakage power dissipations accurately, estimation models have been formulated for all the three logic styles that we have considered in our work.

Based on the realization of large number benchmark circuits, performance of the three logic styles have been compared, in terms of area, delay, power dissipation and energy requirements. The effectiveness of the dual-$V_T$ approach for the three logic styles have also been studied.