Abstract

Image fusion incorporates complementary and redundant information available in input images in such a way that the fused image describes more accurate information than that of any of the individual images. The process of blending several images from various information sources provides extended value to the user. In many applications such as telemedicine, satellite imaging, etc. real-time image fusion is required for efficient analysis. To realise a real-time image fusion system, a series of independently running modules such as registration, fusion and compression are required. Very Large Scale Integration (VLSI) based hardware accelerators for image registration, fusion and compression provide a low-cost solution for real-time image fusion systems.

Image registration is the primary pre-processing step in image fusion. It deals with the alignments of the pixels in the input images. For a complete registration process, both rigid and non-rigid registration modules are required. This dissertation presents a non-rigid registration algorithm and its VLSI architecture. After synthesizing the architecture using Xilinx ISE, the maximum frequency is found to be 174 MHz.

After the registration process, images are subjected to the fusion process. A multi-focus image fusion algorithm combines blurred regions of images obtained by changing the focal length of an image sensor. The Infrared and visible image fusion algorithms assume a linear space invariant model for each of the measurements. The architectures of multi-focus image fusion and IR and visible image fusion are synthesized using Xilinx Field Programmable Gate Array (FPGA) and the maximum frequencies are found to be 221 and 250 MHz respectively.

In real-time image fusion, a series of fused images, which have a lot of redundant data, is generated. In wireless image sensor networks and applications such as telemedicine, security surveillance and satellite imaging it is required to compress the images at the source before these are sent to a central location. Compression of a series of images can be achieved through algorithms for video compression. One of the most computation intensive processes in video compression is the Motion estimation process. An octagonal based motion estimation algorithm and its VLSI architecture are also proposed in this dissertation. The design is synthesized using Xilinx ISE. The maximum frequency is found to be 250 MHz, which is suitable for processing more than 800 frames of Common Intermediate Format (CIF) size images and 35 frames of High Definition (HD) images.

Keywords: Image Fusion, image Registration, Image Compression, Multi-Focus Image Fusion, IR and Visible Image Fusion.