Abstract

The primary objective of the software defined radio (SDR) system design has been fixed for supporting various existing wireless communication standards (2G, 3G and 4G) along with the provision for incorporating the evolving standard (5G), online high definition video and audio streaming and visualizing capability, high speed internet access around the globe with a reduced battery life and reconfigurable capability at the lowest possible cost. In light of the foregoing observation, realization of a SDR system has been attempted in this thesis by designing and developing reconfigurable digital up converter for zero-IF baseband modulator. Therefore, IF processing part in SDR system has been performed using the digital up converter (DUC) and digital down converter (DDC) blocks, which are placed next to the ADC and DAC in the transmitter and receiver paths respectively. The DUC and DDC comprise a digital frequency synthesizer along with interpolator and decimator respectively. However, in order to support different categories of wireless standards, the interpolator and decimator should be reconfigurable in nature. In addition, direct digital frequency synthesizer (DDFS) should have a wide range of spurious free dynamic frequency range (SFDR) support.

The pulse shaping interpolation filter used in the IF processing of some of the popular 3G standards IS-95, WCDMA, UMTS and DVB standards has been analyzed. It is observed that the pulse shaping filter is characterized by different parameters including filter lengths, interpolation factors and roll-off factors for different standards. In this dissertation, two reconfigurable interpolator architectures have been designed and implemented which can change the above mentioned filter parameters at different points of time by simply selecting the proper control signal. These architectures have been designed based on the hardware multiplexed common operator technique in order to achieve better optimization of power, area and speed in case of single chip solution.

In the reconfigurable interpolated FIR filter, reconfigurable multiple constant multiplication (RMCM) blocks are the critical elements which define the overall performance of the desired filter implementation. In this dissertation, three new architectures have been introduced for designing efficient low complexity RMCM design which are based on 2-bit binary common sub-expression elimination (BCSE) algorithm, vertical horizontal binary common sub-expression elimination algorithm (VHBCSE) and canonical signed digit based vertical horizontal common sub-expression elimination algorithm (CSD-VHCSE). The performance analyses of hardware implementation of these RMCM blocks results have been presented to showcase the merits of the proposed architectures over those of the other existing works on RMCM design.

The main challenges in the digital frequency synthesizer are the adjustable SFDR support ability, fine frequency resolution capability, achieving maximum operation frequency along with the reduced spurs generated by phase and amplitude truncation during the phase accumulation. An efficient DDFS with adjustable SFDR range has been implemented in order to fulfill the zero-IF processing in the next generation mobile handset. Successive error approximation algorithm has been introduced for developing the DDFS where the user-selected SFDR range reconfigures the hardware in order to achieve low complexity.

Reconfigurable architectures of other blocks like baseband demodulator, decimator along with encoder/decoder blocks are being left for the future work in this direction. Validation of the desired SDR system with some real time signal is to be carried out after final integration of all of these reconfigurable blocks of the transceiver into a single architecture.

- **Keyword: Software Defined Radio, Digital Up Converter, Multiple Constant Multiplication, Direct Digital Frequency Synthesizer, Reconfigurable Architecture**.