ABSTRACT

In this dissertation, we have designed fault tolerant architectures for real-time signal processing applications using static redundancy and dynamic reconfiguration methods. For systems with structural regularity, dynamic reconfiguration is preferred due to its area and power efficiency. But because of its offline testing and reconfiguration, the method cannot be applied in fault tolerant designs of real-time systems. We have made the testing and reconfiguration online incorporating hot-standby topology in the dynamic recovery technique making it suitable for real-time applications. We have also incorporated some features like graceful degradation, *C*-testability and cascadability in this method to increase its practicability. But for systems where the use of dynamic reconfiguration is impossible or costly, we must opt for static redundancy methods. Most of the existing static fault tolerant approaches suffer from the limitations like voter reliability or high area and delay overheads. We have modified some of the techniques to mitigate their pitfalls and proposed some new defect tolerant approaches those achieve higher fault tolerance with lesser resources compared to the existing methods. We have combined redundancies at various levels to get the benefits of the individuals alleviating their drawbacks. We have also proposed a new fault tolerant technique based on triple transistor redundancy that offers good reliability at minimum increase in area and delay overheads compared to the existing methods and hence is well-acceptable in resource constraint applications. We have proved that for every fault tolerant technique, there exists an optimal granularity value for which reliability is maximum for minimal increase in area and delay overheads. Our fault tolerant motion estimation unit designed by combining various fault tolerant modules offers 224% increase in reliability (with failure probability of single inverter = 10^{-3}) for 136% increase in area overhead, which is much better compared to its triple modular redundant counterpart.

Keywords: Fault tolerance, reliability, dynamic reconfiguration, static redundancy, triple modular redundancy, hot-standby, graceful degradation, *C*-testable, quadded logic, quadded transistor logic, triple-transistor logic, granularity, motion estimation.