Abstract

Analog circuits are fundamentally essential components of today's high performance ICs. There is a pressing need for automation of analog circuit design. However, not too much effort has been spent towards automating analog circuit design. Methods for automation of analog design are yet to be accepted widely in the industry.

In this thesis we propose new methods for (1) Automatic synthesis and sizing of topologies for analog circuits, (2) Application of formal verification techniques like model checking and equivalence checking for validation of transient response of analog circuits, and (3) Simulation based functional verification of full custom digital designs.

We present a scheme for automated analog circuit synthesis which includes topology generation and device value optimization. The scheme is based on the use of Genetic Algorithms (GA) and Particle Swarm Optimization (PSO) techniques. The circuit representation scheme employs a *topological reuse* based approach – it uses commonly used subcircuits for analog design as inputs. The design of the evaluation function for the GA and PSO has also been automated to a great extent. We present several experimental results obtained using this scheme, including two types of comparators, two types of oscillators and an XOR logic gate.

We present a method for verification of transient response of nonlinear analog circuits using model checking and heuristic search. We propose a new temporal logic called Ana CTL which is suitable for specifying properties of analog systems. The transient response of a circuit under all possible input waveforms is represented as a discrete finite state machine (FSM). We have developed algorithms to run Ana CTL queries on this discretized model using heuristic search based methods, which reduce the run time considerably by avoiding creation of the whole FSM. We also present methods for checking the equivalence of transient response of two analog circuits. We have introduced a notion of *approximate* equivalence. A query language for checking different notions of user definable *approximate* equivalence has been presented which extends the syntax of the Ana CTL model checking language.

Custom digital circuits are designed at transistor level and hence pose the same type of challenges as analog circuits in terms of design and verification effort. We present a new switch level simulator *Natsim* which can be used to simulate custom digital designs for which other simulators fail. We have developed a robust voltage and delay calculation algorithm which enables *Natsim* to correctly simulate complex designs. A methodology for simulation based functional verification of memories and other custom cells has been proposed. We present verification results for several types of memory designs using a wide range of technologies.