# Abstract

The estimation of timing behavior efficiently and accurately is a challenging task due to the complexity of present day circuits. In this thesis, we propose a comprehensive symbolic event propagation (SEP) methodology for analyzing the timing behavior of digital circuits at the gate level and show that the same methodology can be used for solving several timing related problems. In SEP, the inputs are initialized with appropriate events and these are then propagated through gates in a symbolic manner taking account the functional and the temporal behavior of the gates. The proposed methodology is generic and has been applied to solve several timing related problems like timing analysis of sequential circuits, statistical static timing analysis, timing optimization and delay fault testing.

We apply the proposed methodology for analyzing the timing behavior of sequential circuits more accurately considering combinational and sequential false paths as well as other important issues like triggering of traditional false paths due to multiple input switchings, simultaneous switching. This provides an accurate estimate of the critical delay. We propose a few resource constrained techniques to determine good upper bounds on the critical delay for large circuits.

For statistical static timing analysis, we first show that traditional Monte Carlo (MC) simulation often overestimates the critical delay compared to MC simulation using SEP when the gate delays vary stochastically. We present a viable scheme that combines SEP with statistical timing analysis thereby achieving a significant level of accuracy within acceptable computational overheads.

We propose a new scheme for improving the performance of synchronous sequential circuits. In this scheme a circuit is driven by an adaptive clock that provides two different clock frequencies. One of them is the conventional clock and the other, having a shorter period, is applied when the circuit stabilizes to its final value well before the critical delay. We use SEP to analyze the timing behavior of synchronous sequential circuits and provide add-on circuitry to select the appropriate clock based on the current state of the circuit.

We introduce additional constraints in the SEP methodology to generate hazard free tests for robust path delay faults. This approach identifies all robustly testable paths in a circuit and the corresponding complete set of test vectors. We address the problem of finding a minimal set of test vectors that cover all the robustly testable paths. Greedy and simulated annealing based algorithms have been proposed to find the same.

We perform experimentation on ISCAS89 benchmark circuits. We obtain more accurate results at reasonable amount time for the different timing related problems. In this thesis, we show that symbolic event propagation methodology can be used in an unified way for analyzing a variety of timing related characteristics of circuits at the logic (gate) level.