Abstract

Today's feature-laden portable electronic devices require multiple supply voltages for minimizing the cross-talk among the different functional blocks/subsystems. Low dropout regulators (LDRs) are often preferred to generate a noise-free/clean, accurate, well-regulated output voltage for low power applications. Based on the presence of an off-chip output capacitor, the LDRs are classified into two categories. A with-capacitor LDR (WC-LDR) provides a tight voltage tolerance band during load transient edges at the expense of an extra off-chip component and IC pin-count. On the other hand, the capacitor-less LDR (CL-LDR) offers a better integration possibility with a small PCB foot-print and less IC pin-count. However, the amount of overshoot/undershoot for sudden load variations is relatively high due to the absence of the off-chip capacitor at the output.

In this dissertation, we have explored both the above categories of LDRs to cater to different requirements of portable devices. To improve the battery lifetime, one has to minimize the quiescent current without compromising the transient response. In view of this, an adaptive biasing scheme is primarily adopted. In addition to that, a self-compensated architecture is proposed to cover a wide dynamic range of load current for stable operation.

To start with, the widely used nested Miller compensated (NMC) architecture is revisited to identify the various design trade-offs and limitations. A systematic design procedure is also proposed to optimize various dynamic performances. After that, a self-compensated architecture that has many advantages over the NMC one is developed. Using this architecture a generic, adaptively biased LDR (AB-LDR) topology which is suitable for both the with-capacitor and capacitor-less conditions is proposed. A power efficient enhanced current mirror (ECM) buffer is proposed in particular to the WC-LDR to expand the loop bandwidth of the regulator. We have also proposed a dynamically slew enhanced adaptive bias (DSE-AB) scheme to improve the dynamic response further in the WC-LDR. Finally, while applying the DSE-AB scheme in the CL-LDR, an issue of low momentary damping is observed as various system poles move at different rates during transient. A current-limited DSE-AB scheme is explored to increase the momentary damping in capacitor-less condition. All the topologies are developed, backed with theoretical analysis and validated with simulation and experimental results when they are implemented in a standard 0.18 μm CMOS technology.

Apart from exploring different topologies, this dissertation has also proposed advancement in small signal analysis of the adaptively biased LDR (AB-LDR) topologies. In any AB-LDR, there are two feedback loops present in the system, namely the main feedback loop (MFL) and the adaptive bias loop (ABL). Here we consider the interaction of these two loops to derive the stability margin. Also, the impact of the ABL on improving the dc load regulation is explained from the small signal analysis. We have derived the small signal transfer functions of both the loops taking into account the interaction with the other loop. Those transfer functions accurately predict the small signal stability as well as justify the improved dc load regulation.

Keywords- Low dropout regulator, voltage buffer, current mirror, Q-peaking, main feedback loop, adaptive bias loop, nested Miller compensation, with capacitor regulator, capacitor-less regulator, dynamic slew enhancement, adaptive biasing.