ABSTRACT

Fractal image coding has drawn the attention of many researchers owing to its several desirable properties including high compression ratio, reasonably good image quality at low bit rate, fast decoding and resolution independent nature. A major objective of the research work embodied in this thesis has been to tackle the computationally intensive fractal encoding problem by exploring parallelism inherent in the algorithm and by adopting of hardware based approach towards its solution. The present work not only aims at enhancing the encoding speed but also attempts to limit the hardware cost in terms of memory utilization, reduces the software dependency by avoiding the pre-processing operations and modifies the algorithm to improve the compression ratio as well as the image quality. To speed up the encoding process, which consists of block-wise image segmentation, affine transformation, and computation of relevant parameters and similarity measure, parallel processing and pipelined operations have been incorporated in the proposed architectures. The present research has conceived and developed speed enhancing algorithm, that in addition to limiting the search area, succeeds in retaining the image quality while operating at a fast compression rate. Moreover, hybrid fractal-SPIHT architecture has been designed to improve the performance of the pure fractal encoder. Additionally, a simple decoder module based on adaptive partitioning scheme has been implemented to obtain the reconstructed image.

Keywords: Fractal Image Compression, Affine Transformation, Attractor, Iterated Function System, Quadtree Partitioning, FPGA, Parallel Processing.