ABSTRACT

The search for a cost effective interconnect architecture and increasing communication demand in Systems-on-Chip (SoC) designs have paved the route to Network-on-Chip (NoC) research a decade back. The Network-on-Chip (NoC) communication architecture is a packet based network where cores communicate among themselves by sending and receiving packets. High parallelism, smaller latency in data transmission and facility of Intellectual Property (IP) re-use have made NoCs overcome the problem of bandwidth and latency in conventional bus-based interconnects. However, like all other designs, NoC based SoC designs must also be tested for defects. Survey of different test techniques developed for NoC based systems suggest that focus has been primarily on finding improved test techniques for NoC based logic cores. However, the embedded memory content in NoC based systems have increased over the years and will continue to increase. Due to their high density, these embedded memories are more prone to defects than other type of on-chip circuits and therefore, require more importance when it comes to testing NoC based systems. In this thesis, the objective has been to devise cost effective test techniques for memory modules in a NoC based memory system, targeting minimum area overhead at optimized test time and test power. The research was aimed at improving the existing approaches of test of NoC based memory cores along the following directions : test architecture, test scheduling algorithms and on-line test techniques. A distributed test architecture has been proposed to allow hardware sharing and eventually reduction of Design-For-Testability (DFT) area overhead. The test technique utilized by the test hardware tries to incorporate the advantages of both parallel and serial approaches of testing embedded memories, thereby reducing the test time. For the test architecture proposed in the thesis, a test scheduling algorithm has been proposed focusing on limiting the number of concurrent test blocks under power constraint with the aim of performing a power aware test of the memory cores. Experiments performed on ITC'02 benchmark circuit confirms that our proposed test schedule performs a more power constrained test as compared to dedicated Built-In-Self Test (BIST) techniques for embedded memories.

In addition to improvement of existing approaches, novel test architectures have also been devised. These architectures involve utilization of the existing on-chip resources, such as refresh circuit for test purpose. The refresh based test technique has been effectively utilized to perform on-line tests of embedded DRAMs interconnected by the NoC infrastructure. To perform the on-line tests, transparent March tests have been used in place of standard March tests, to ensure restoration of initial contents of the memories after test. Reusing refresh allows

periodic testing of DRAM without interruption while overcoming the requirement of additional Design-For-Testability (DFT) hardware. Analytic results have been used to explore the fault coverage of the proposed test technique. The transparent test technique has also been employed for detection of permanent faults developed in FIFO buffers during field operation of NoC. A prototype implementation of the proposed test algorithm has been integrated into the router-channel interface and the on-line test has been performed with synthetic self-similar data traffic. The performance of the NoC after addition of the test circuit has been investigated in terms of throughput using a System C based NoC simulator. Area overhead of the test circuit has been studied by synthesizing the test hardware with a industry standard design library.

To summarize, the research work presented is an attempt to provide system-level solutions for effective power constrained testing of hundreds of embedded memories connected using NoC with low overhead in Design For Testability hardware.