ABSTRACT

Beginning with algorithm specification by a set of recurrence equations, the thesis examines synthesis problems of systolic and enhanced systolic arrays. Among the enhanced systolic arrays, the Instruction Systolic Array has been studied in detail and a new architecture, called the Tagged Systolic Array, has been introduced. The usefulness of these architectures have been demonstrated by deriving designs for a number of problems from different application domains such as matrix operations, digital signal and image processing, searching and sorting, computational geometry, graph theoretic algorithms etc. A computer aided design tool has been developed for automated synthesis of instruction and tagged systolic arrays. This tool uses heuristic based algorithms at different stages of the design. A rule based approach has been used in this tool for selection of a proper combination of heuristics based on the problem under consideration. It has been shown that the CAD tool often produces a design with performance close to a carefully handcoded design. Finally, partitioning of a problem and mapping a partitioned problem on a mutiple array architecture have also been discussed. The results derived are applicable to both ordinary and enhanced systolic arrays.

Keywords (with CR classification)

A.2.1 & A.5.1 : Design styles (Parallel, Pipelined)

A.7.1 : Types and design styles (Algorithms implemented in hardware, VLSI)

B.0 : General (Instruction set design, System architectures)

B.1.2 : Multiple data stream architectures (Array and vector processors, Parallel processors)

B.3 : Special-purpose and application based systems

F.1.10 : Numerical analysis (Miscellaneous)

F.2.2 : Graph theory (Graph algorithms)

H.4.10 : Image processing (Miscellaneous)

H.2.1 : Applications and expert systems

I.6 : Computer aided systems (Computer aided design)