Abstract

Implementation on parallel computers is the only way to meet the application demands of artificial neural networks. And, the choice of an appropriate mapping scheme is vital for the implementation of neural network algorithms in parallel processing environment. In this thesis, new improved mapping schemes have been presented for the efficient execution of neural network models on parallel computers. Specifically, four different parallel architectures, such as: fine-to-medium grain SIMD (Single instruction multiple data stream) computers, distributed memory multiprocessors (DMMs), systolic arrays, and massively parallel hierarchical computer systems, are comsidered for the proposed implementation of neural network algorithms. The mapping schemes have been illustrated on two popular neural network models, i.e, the Hopfield model and the multilayer perceptron with back-propagation learning.

As neural networks were inspired by the parallel nature of the processing involved in the human brain, they have a number of parallel aspects embedded in their structure. Each of the proposed mapping schemes has used a different parallel aspect to parallelize the neural network computations, so that the parallel aspect chosen is most suitable to the concerned parallel architecture. For each of the mapping schemes, an analysis is presented to estimate the efficacy of the mapping scheme. This is done by predicting the P processor speedup and its variations with both the size of the neural network and the number of processors.

Keywords: *multilayer perceptron, Hopfield network, back-propagation algorithm, recall phase, learning phase, processor array, initial data assignment, data routing, dependency graph, speedup performance, scalability.*