ABSTRACT

The present thesis embodies Genetic Algorithm formulations for a number of hard graph optimization problems. The philosophy of Genetic Algorithm as an efficient optimization tool, is first presented. The design aspects of different components of the Genetic Algorithm are next discussed. A new reproductive plan which offers a performance improvement for the Genetic Algorithm is proposed. Genetic Algorithms for six hard graph problems *(Embedding of a complete graph in a minimum sized hypercube, Rendering a graph bipartite by minimum node deletion, Graph coloring by minimum colors, Obtaining an optimal cover of cliques of a graph, Obtaining optimal set cover and weighted set cover of some items. and Determining an optimal permutation of some objects)* have been formulated. The experimental results indicate the superiority of the Genetic Algorithm over the different heuristic methods, and the simulated annealing method. The Genetic Algorithm formulations for these graph problems have been employed for solving a number of application problems *(Encoding of the symbolic states of a Finite State Machine, Port assignment of 2-port memories, Scheduling of Test plans, Determining Testing cost of a Built-In-Self-Test scheme, Programmable Logic Array folding, and Gate matrix synthesis)* which are encountered in various phases of VLSI design. For the optimal permutation problem, a distributed parallelization scheme is adopted for the Genetic Algorithm. Various aspects of the parallel Genetic Algorithm have been studied. The experimental results indicate performance improvement of Genetic Algorithm by parallelization. The advantage of employing this parallel scheme of Genetic Algorithm for hard optimization problems of a class with separable constraints has been shown, and substantiated by the experimental results.

Keywords : Genetic Algorithm (GA), Graph problems, Embedding, Node partitioning, Bipartite graphs, Set cover, Simulated Annealing (SA), Finite State Machine (FSM), Very Large Scale Integrated circuit (VLSI), Built-In-Self-Test scheme (BIST), Programmable Logic Array (PLA).