Abstract

Among available architectures of analog-to-digital converters (ADC), pipeline architecture is the most popular one because of its wide-spread application and ease of implementation. A pipeline ADC contains several identical coarse stages connected in cascade. Due to their coarse nature, these stages provide an optimum balance of sampling speed, power consumption and resolution of the ADC. Since an ADC is characterised by these three major performance metrics, a pipeline ADC can produce a very impressive figure-of-merit (FoM), which is indicative of its superiority over other topologies. Primary objective of this thesis has been to improve the performance of a pipeline ADC by applying numerous enhancement techniques on it, which can lead to a better FoM. Sampling speed of a pipeline ADC can be enhanced by using time-interleaving and double sampling techniques. Double sampling technique reduces the power and die usage of the ADC as well. Careful selection of pipeline stage resolution can manage the number of stages along with gain and bandwidth of the stage amplifiers. Power reduction is possible by removing the front end sample-and-hold amplifier, which approximately consumes as much power as a front end pipeline stage. A 7-bit 75 MSPS pipeline ADC has been implemented in a 0.18 μm CMOS process, consuming only 73 mW of power, using the aforementioned enhancements. Further improvement of ADC performance is possible by applying calibration algorithms. ADCs with low amplifier gain and small capacitor size can help to reduce the power and die area consumption considerably. However, such amplifier and passive components produce distorted ADC output, lowering its linearity. The non-linearity produced can be removed efficiently by calibration techniques, thus providing improvement in all the metrics of a pipeline ADC. Two digital foreground calibration algorithms, both based on radix extraction principle, have been proposed in this thesis, supported by behavioural simulations, circuit simulation and Silicon implementation.

Keywords- Pipeline ADC, time interleaving, double sampling, bottom plate sampling, digital error correction, digital calibration of pipeline ADC.