Abstract

Manufacturing test screens out bad chips during the Integrated Circuit (IC) design and production process. Diagnosis is used to find out the reason behind the failure. Diagnosis is especially important when the yield is low or when a customer returns a failed chip. Failure analysis relies on a logic-level process, known as fault diagnosis. It uses the observed failing responses and the structure of the circuit under diagnosis (CUD) to search for locations that are potentially faulty. Information provided by this logic diagnosis process is used to guide physical observation of the circuit during failure analysis. However, with the increasing complexity of ICs, physical inspection in today's multilayer deep submicron devices has become exceedingly expensive and time consuming. Therefore, improving the efficiency and accuracy of fault diagnosis is necessary for the yield ramping up. The quality of diagnosis impacts directly the time-to-market and the total product cost. Like almost every aspects of testing, diagnosis is a well studied area. Most of the studies on diagnosis have assumed a single defect. However, for present technologies and chip sizes, this assumption may not be true. Often, multiple defects in a failing chip better reflect the reality. A chip can fail the manufacture test set due to defects that can be present anywhere in the flip-flops (FFs), combinational logic, or even the design for testability (DFT) circuitry (such as scan chains). This thesis addresses diagnosabilty issue in both combinational logic as well as scan chains. Initially a multiple fault diagnosis technique based on multiple fault simulation has been developed for combinational logic diagnosis. The proposed approach can diagnose upto ten simultaneous faults within moderate time. A Diagnosability metric that can accurately measure the diagnostic power of a test set has also been proposed. The metric can be utilized to increase the diagnosbaility of a test set. Two different techniques (a hardware based one and a software based one) have been developed to diagnose scan chain faults. The proposed strategies can successfully identify the failure locations of a bad chip within moderate time and without incurring extra costs.

Keywords: Combinational Logic Diagnosis, Diagnosability Metric, Design for Diagnosis, Scan chain diagnosis