Title of PhD thesis: Prediction and Reduction of ReferenceSpur in a Frequency Synthesizer

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Abstract of the thesis:

In a wireless communication system, inclusion of more features requires higher spectralpurity of its local frequency synthesizer. In a phase locked loop (PLL) based frequencysynthesizer, the ripple present at the control voltage input of its voltage controlledoscillator (VCO) modulates its output frequency and generates spurious tone of thereference frequency (known as reference spur). The spur generated at the output ofthe frequency synthesizer degrades the signal-to-noise ratio (SNR) at the receiver ofthe system. The work in this thesis includes prediction and reduction of spur in aPLL based frequency synthesizer. The first part of the thesis presents an analyticalapproach for accurate prediction of the reference spur. In this approach, effects of PFD-CP (phase frequency detector - charge pump) non-idealities and leakage have been considered. Transistor level SPICE simulations show that using the proposedapproach, the error in predicted spur has been reduced from 29.84 dB to 0.64 dB. The proposed approach has been extended to predict the spur in frequency synthesizerarchitectures having pulse repetition (PR) based spur reducing technique.

In the second part of the thesis, phase locked loop based frequency synthesizer architecture to reduce the reference spur has been proposed. In the proposed architecture,an array of switched capacitors and a delay locked loop have been used toevenly transfer the charge from the charge pump to its loop filter at a fixed number of equi-spaced time intervals. As a result, the fundamental and higher-order harmonicsof the reference spur are reduced. To reduce the effect of element mismatch onthe spur reduction, a randomization block has been incorporated in the architecture.Stability and phase noise of the proposed architecture have been analyzed. The proposedarchitecture including randomization block has been designed in 180 nm CMOStechnology. Measured result shows that the spur is reduced by 17.64 dB, 11.85 dB,13.40 dB, 20.68 dB and 12.25 dB, respectively, for the fundamental, 2nd, 3rd, 4th and5th harmonics with respect to those of a conventional architecture.

Keywords- Reference spur prediction, reference spur reduction, periodic charge distribution,pulse repetition technique, frequency synthesizer, phase locked loop (PLL)