Abstract

The present thesis embodies the applications of Cellular Automata (CA) for designing reliable and testable VLSI circuits. The homogeneous structure of CA and its different phases of development are briefly reviewed. The theory of generating Error Correcting Code (ECC) with the help of CA has been investigated. Different encoding and decoding schemes for detecting/correcting random bit errors and byte errors have also been proposed. In both the cases it is shown that the hardware implementation of the decoding schemes are simple as well as cost effective. Further, an elegant scheme is derived for designing Single-Error-Correcting, Double-Error-Detecting and All-Unidirectional-Error-Detecting (SEC-DED-AUED) codes using a special class of non-group CA. Employing the inherent properties of the same non-group CA, a novel scheme for synthesizing easily testable finite state machines (FSM's) is presented. A BIST structure is proposed for testing memory array, where the CA is mainly used as a pattern generator for testing Pattern Sensitive Faults (PSF's). Two-dimensional (2-D) CA have been characterized based on the elegant matrix algebraic characterization of 1-D CA. This 2-D CA is used as a pseudo-random pattern generator. Better randomness of the patterns generated by 2-D CA over that of 1-D CA and LFSR has been established. Exploiting this better randomness property of 2-D CA, the design of pseudo content addressable memory has been proposed.

Keywords : Cellular Automata, VLSI, Error Correcting Code, Synthesis for Testability, Built-In-Self Test, Pseudo-Random Testing, Associative Memory.