CHAPTER 1

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The advancement of integrated circuit technology has brought-in phenomenal changes in the design, production and maintenance of digital systems. With the ever-increasing density of circuit packaging, the problems of fault diagnosis have taken new dimensions. Higher packaging density has substantially increased the amount of circuit information to be stored for the purpose of fault diagnosis. The restriction on the pin-count of these high density chips has considerably reduced the access to the internal lines of the circuit. As a result, the overall controllability and observability of the network implemented on a chip has greatly reduced. This reduction necessitated extensive processing of the information collected during a fault-diagnosis experiment. Consequently, the complexity of test generation and test execution have greatly increased. The cost of testing gradually formed sizable portion of the product development, manufacturing and maintenance costs. In view of this situation, considerable attention is paid to the formulation and implementation of efficient test generation algorithms and diagnostic procedures. The emphasis is directed towards reduction of the cost in terms of diagnostic information storage and the associated computational effort. Ultimately, it is deemed necessary to

pay due attention to design the circuits such that they are testable within a stipulated cost constraint.

The major functions of a fault diagnosis procedure are (i) analysis of the network behaviour and generation of a test-set, (ii) test application, and (iii) process the test response for detection/location of faults. These functions involve a large number of tasks such as fault modelling, simulation, testability analysis and test generation, test-set optimization, fault location etc. A review of the state of art (outlined in the subsequent chapters) reveals that wide-ranging methodologies have been proposed to handle each of these tasks. Further, the network modelling and analysis varied considerably for each of these tasks. In this background, it is felt necessary to evolve a model best suited to handle all these tasks with uniformity and consistency. With this objective as one of the prime considerations, a graph-theoritic model termed as "Diagnostic Logic Graph (DLG)" is proposed in the present work. The DLG model is used in conjunction with six-valued logic for circuit-level fault diagnosis. Throughout the work, stuck faults of permanent nature are considered in connection with irredundant logic networks. Using this single model, following aspects of fault diagnosis are dealt with in the present work - true-value simulation, fault coverage evaluation, computation of minimal/nearly minimal test-count, adaptive test generation, fault location, and, testable design of digital networks. This single model used for the representation of combinational

circuits is adapted to handle sequential circuits and MOS circuits. Further, same DLG model is extended to handle system-level fault diagnosis. The following paragraphs briefly outline the contents presented in the subsequent chapters.

The Chapter 2 deals with combinational circuits. Following a brief review of state of art for test generation and fault simulation, the new DLG model is introduced. Based on various properties of this model, a procedure is described to perform true-value simulation. Later, a method of fault-coverage evaluation is formulated. This eliminates the usage and maintenance of exhaustive fault-dictionaries and study of fault-collapsing aspects that are considered for conventional fault simulation methods. Following this, computation of test-set size is described using the concepts of test-count. Two single-fault detection test-set generation procedures are presented considering the path-sensitization principles, based on (i) test-count for the circuit, and, (ii) adaptive test generation with a start-small approach using terminal-stuck fault detection test-set. Further, multiple-stuck fault location aspects are discussed with referrence to achieving forced consistency in observed response and formation of fault matrices. Lastly, the order of complexity involved for the computation of various procedures formulated in the chapter is discussed. Some of these basic procedures are used in the later chapters.

In Chapter 3, the DLG concepts are extended for representation of sequential circuits. Test generation for

single-fault detection and location of multiple-stuck faults are dealt with. Chapter 4 discusses the usage of DLG for MOS circuit testing. Switching device faults and charge retention concepts are appropriately represented and a solution-graph is developed out of DLG to generate stimuli for initialization and testing purposes. An adaptive test generation procedure is formulated to cover all types of stuck faults concerning transistors, bus-lines, and, primary-input/primary-output lines.

In Chapter 5, testable design of combinational circuits is discussed. A general method of modification of circuits to achieve two-pattern testability is introduced considering terminal-stuck faults. Also, implementation of adhoc modifications for certain circuits is discussed on case to case basis for reduction of terminal-stuck fault test-set size. Further, placement of test-points and a partitioning strategy for generation of a test-set with reduced size is introduced. This is done with a view to provide complete internal fault coverage. A divide and conquer testing strategy is, next, proposed for multiple-fault detection of circuits using single-fault detection test-set. Adaptation of DLG for system-level fault diagnosis is reviewed at Chapter 6. A design for interconnection links of a distributed system network is formulated. Distributed diagnosis algorithm is developed for this network to locate faulty modules provided total number of faulty modules in the system does not exceed a specified limit.

It is evident from the above discussion that an endeavour is made towards formulation of a unified approach for fault modeling and simulation of digital networks including MOS circuits and system level diagnosis. The same methodology is used for testable design of circuits. Considerable advantage is derived by using DL graph with respect to uniformity in treatment of all aspects of fault diagnosis such as simulation, test generation, fault coverage evaluation and fault location.