ABSTRACT

On-chip communication is being regarded as one of the most important issues in System-on-Chip (SoC) design. Network-on-Chip (NoC) has evolved as a viable alternative to the bandwidth limitations of bus-based SoCs. NoC consists of a router fabric connected in certain fashion. Intellectual Property (IP) cores, carrying out application tasks are attached to individual routers. A major challenge in the overall NoC-based system design is to associate the IP cores with the routers. This is commonly known as the process of application mapping. Given an application, represented in the form of a core graph, application mapping problem is to attach individual cores realizing each task to a router. The performance of the overall system is naturally dependent on this mapping. To reduce communication cost, communication time and energy, it is desirable to keep the distances between highly communicating cores small. This thesis reports a number of efficient mapping techniques for NoC design. Various avenues that have been explored include *(i)* iterative mapping algorithm using Kernighan-Lin (*KL*) bi-partitioning, *(ii)* a constructive heuristic, *(iii)* a Discrete Particle Swarm Optimization (*DPSO*) based meta-search technique, and *(iv)* a thermal uniformity-aware strategy for application mapping. Apart from the conventional mesh topology, mapping problems on other well-known topologies, such as, Mesh-of-Tree (MoT) and Butterfly-Fat-Tree (BFT), have also been addressed. The proposed techniques show reasonable improvement in communication cost while considering static operation of the system. There is also improvement in dynamic performance and energy consumption of the solutions produced, compared to the best ones reported in the literature. To see the optimality of the mapping techniques, Integer Linear Programming (ILP) formulation has been made. It has been found that the mapping techniques produce similar results as in ILP with less CPU time. The mapping strategies show better improvements particularly for NoCs having large number of cores. While communication cost reduction dictates highly communicating cores to be mapped in close vicinity, the thermal-uniformity viewpoint also needs to be considered. Irregular heating across the chip can cause creation of local hotspots and delay variations. The thesis also proposes a thermal uniformity-aware mapping with limited degradation in communication cost.

KEY WORDS: Network-on-Chip (NoC), System-on-Chip (SoC), Application Mapping, Mesh, Mesh-of-Tree (MoT), Butterfly Fat-Tree (BFT), Kernighan-Lin (*KL*) Partitioning, Constructive Mapping, Particle Swarm Optimization (*PSO*), Thermal Uniformity-Aware Mapping.