ALGORITHMS AND ARCHITECTURES FOR ESTIMATION OF RADAR PULSE PARAMETERS IN MODERN ELECTRONIC SUPPORT RECEIVERS

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Abstract

There are several challenges in designing modern electronic support (ES) receivers to meet today's electronic warfare (EW) needs. In this dissertation, we first consider one such problem, namely, that of estimating direction of arrival (DOA) of radar pulses using base line interferometer (BLI) from "size weight and power" (SWaP) optimisation aspects. For SWaP-optimised BLI, switched-mode operation with a fewer number of receiver channels is preferred. Such switched-operations, however, result in sub-optimal performance. To overcome this, we propose a three antenna BLI algorithm named as "co-operative BLI" (Co-BLI), which provides more phase error margin while maintaining at par high DOA estimation accuracy. To increase estimation accuracy further, we next extend it to the case of more number of antennas and propose a novel way to optimise them. For real time operation, we develop a "mapping-based co-operative ambiguity table" (M-CAT) - a look-up table based scheme facilitating high throughput implementation while avoiding complex computations. The proposed algorithm has been validated through MATLAB simulation and implemented in FPGA-based real time hardware.

Next, we consider the problem of combating delay error effects in delay line (DL) based sub-Nyquist estimation of the frequency of intercepted radar-pulses in wide-open mode. We propose a two DL approach where a shorter DL produces a coarse estimate of the frequency which is used as a reference by a longer DL to produce more accurate coarse estimate. This is followed by a fine estimation producing 100 % accurate (in absence of noise) estimate. To tackle the case of larger delay error, this approach is extended to a multiple DL model. We validate the proposed methods both by MATLAB-based simulation and by developing prototype hardware.

Lastly, we consider the problem of architectural optimization for throughput maximization in adaptive EW, in particular for adaptive filters. For this, we use a "constrained minimally redundant radix-4" data format that provides an alternate sparse representation of 2's-complement data. Using these, the filtering and weight update modules are worked

out, leading to adaptive filter architectures with a shorter critical-path than the original. To reduce hardware complexity, we use systolic mapping to obtain a bit-parallel digit-serial and bit-serial digit-parallel architectures. We conclude this treatment by proposing efficient architectures for adaptive filters using distributed-arithmetic.

Keywords: Electronic Support, Base Line Interferometer, Direction of Arrival, Sub-Nyquist Sampling, Delayline, Constrained Minimally Redundant Radix-4 Data Format, Adaptive Filter, Distributed Arithmetic.