ABSTRACT

Power dissipation during test has been found to be much higher than during normal mode of operation. This has led to the power aware testing strategies. Many of the existing low power testing approaches concentrate on reducing transitions in the circuit. This minimizes the dynamic power consumption. However, an efficient power reduction technique should consider reducing the leakage power as well. Test set volume is another significant parameter that plays a major role in the selection of test pattern set. Hence, a suitable trade-off between test volume and power is an important criterion in testing low power devices. Along with total power dissipation, temperature profile across the die is an important aspect of low power testing. Peak temperature is a function of both heat generated from the circuit and heat dissipated to the ambient air. Spatial temperature non-uniformity has a non-uniform effect on relative path delays within logic blocks. Thus, thermal aware testing strategies demand specialized schemes to address these issues. This thesis proposes a number of strategies for power- and thermal- aware testing of digital circuits. The proposed techniques include a customization of given pattern set into a low power test set, power- and thermal-aware test vector reordering and don't care filling techniques, and a power-aware pseudo-exhaustive internal testing scheme based on Cellular Automata. The conventional testing strategies applied to combinational and sequential circuits are not effective for specialized architectures like memory. *March* tests are found to be the most suitable solution for memory devices. Generation of *March* test sequence is a highly computationally intense exercise. This thesis proposes a fast generation scheme for low power, high fault coverage *March* tests. We also look into a possible modification to the SRAM architecture to aid low power memory testing.

KEY WORDS: Test set relaxation, Don't care fill, Vector reordering, Particle Swarm Optimization, Vector compaction, Low power testing, Thermal aware testing, Memory testing, Built-in-self-test, Cellular Automata, Circuit partitioning

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