Abstract

Memristor, the fourth fundamental passive circuit element, has piqued the interest of researchers due to its unique properties that are suitable for *in-memory computing*. Unlike conventional computing systems that require data transfer between the CPU and memory, in-memory computing architectures provide storage and computation in the same hardware unit. Nowadays, applications of neural network can be found in almost every portable device for image, audio, and video processing. The core computation that is carried out in neural networks, both during the training and the classification phases, is the *Vector-Matrix Multiplication* (VMM). It has been observed that the VMM operation can be performed efficiently in memristor crossbar. When such a crossbar is used for neural network applications, the memristor cells act as synapse, storing the weights of the network in the form of resistance. The in-memory computation capability allows memristor weights to be changed without requiring data transfers. As a result, by directly performing VMM operations and eliminating the need for explicit data transfer, the crossbar can accelerate neural network operations. However, memristor technology is still in its early stages, and faces a number of technological challenges that prevent it from being used effectively in many applications.

The present work addresses various technological challenges associated with memristor crossbar architecture that prevent its effective use in neural network applications. The storage mechanism of memristors is different, which necessitates the use of a new training algorithm compatible with this technology. A training algorithm compatible with memristive technology has been proposed to train neural network applications using memristor crossbar. The crossbar is prone to high number of faulty cells, which can impact the computation of VMM. Thus, an analysis of the impact of faults in applications trained in memristor crossbar is presented, followed by an efficient fault diagnosis approach. Next a fault tolerance approach is proposed to minimize the impact of faulty cells in the overall computation of VMM without sacrificing the inference quality. The experimental results obtained by running various benchmarks and simulations under the Cadence Virtuoso Environment are used to validate the various solutions proposed in this thesis. The experiments conducted demonstrate the effectiveness of the proposed approaches over prior state-of-the-art techniques.

Keywords: Memristor, Crossbar, In-Memory Computing, Neural Networks, Training Algorithm, Fault Diagnosis, Fault Tolerance.