Abstract

The use of deep submicron technologies presents several new challenges in the areas of CMOS devices and circuits. A significant body of the present work has been devoted to identifying and investigating modeling and design challenges in nanometer technologies. In this thesis, we address the development of a technology compact semi-analytical model for nanoscale devices (MONAD) valid in nanoscale region by focusing on carrier mobility. The model is verified due to its proximity to experimental and TCAD simulator data. Further, emphasis is given for the development of analytical models to compute the supply current, delay, and power of a deep submicron CMOS inverter by using MONAD. These models are validated for a series of CMOS technologies (up to 50 nm), for a wide range of inverter sizes, input transition times, and capacitive load. The power delay model is incorporated into the transistor sizing problem and is solved by non-linear programming approach. The accuracy of performance prediction in the sizing algorithm is verified against detailed SPICE simulation results. Further, a novel design methodology is explored for the optimum performance of cascaded CMOS buffer by using MONAD. The accuracy of performance prediction of optimum transistor sizes and scale factor for minimum power-delay and area is verified due to its closeness to Specter SPICE and PSPICE simulation results. The recent explosion in demand for scaling down of technology necessitates the study of different logic families for high speed and low power applications, which is also addressed in this work.

Key Words: MONAD, Carrier mobility, High field effects, Scattering effects, Analytical model, Delay estimation, CMOS Inverter model, Peak supply current, Power estimation, Power-delay model, Transistor sizing, Geometric programming, CMOS Buffer model, CPL,TGL.