line design and achieves significantly high resolution with low power consumption and requires a small silicon area. The dual mode error control digital compensator is implemented to improve the dynamic response of the digital controller.

The proposed design has been verified using standard 0.5μm CMOS technology. The delay line ADC is fabricated with discrete components and the operation of the complete closed loop system has been verified in an experimental setup built on Altera DE2 FPGA based platform. Experimental results validate the operation of the proposed *MBDS* delay line ADC integrated with a digital PWM controller. The PWM controller meets a wide regulated output voltage range of 1.6 V to 3.3 V. The *MBDS* delay line ADC achieves a fine resolution of 27 mV - 30 mV. In-order dual stage digital conversion time is less than 500 ns and 16 digital outputs cover the entire conversion range of 1.6 V to 3.3 V. The proposed delay line ADC reduces chip area by 33% in comparison with a 64 tap delay line ADC and consumes low average current of 66 μA at 3.3 V. Dual mode error control provides improved dynamic response, with a settling time less than 10 μs for a 1 V step change with the voltage mode, digitally controlled 1 MHz buck regulator.

The second proposal presents a new class of digital controller architecture for DC-DC converter to provide wide range of regulated voltage for a wide range of target operating clock frequency. An optimized design of a delay line based ADC and a novel formulation of digital error value have been proposed. In this proposal, digital error value is generated based on target clock frequency and the regulated output voltage. The proposed design of delay line based ADC has been implemented in standard 0.5μm CMOS technology and a prototype has been constructed with discrete components. Complete closed loop operation has been verified in an experimental setup built on an Altera DE2 FPGA based platform. Experimental results validate the operation of the proposed delay line ADC in an integrated digital PWM controller. The optimized design of the digital controller achieves fast dynamic response over a wide target frequency range (6 MHz - 16

MHz) to provide corresponding regulated output voltage in the range of 1.6 V - 3.2 V with a 12.5 mV regulation. ADC Conversion time equals to one clock period of the target frequency. The proposed delay line ADC occupies only $0.08mm^2$ on-chip area and consumes an average current of 6 μA at 2.4 V. The digital loop provides better dynamic response with a settling time less than 10 μs for a 1 MHz target frequency step change.

The third proposal presents a simple dual mode, edge-triggered hybrid DPWM. Dual mode operation of the hybrid DPWM has been introduced to reduce dynamic power consumption of hybrid DPWM and to improve dynamic voltage regulation during transients. The two-clock-domain architecture of the hybrid DPWM has been used for generation of two switching frequencies. Internally self-clock generation circuit uses 8 D-flipflops and fits into one logical element (LE). The self-clock generation circuit occupies a small area and outputs a clock with maximum frequency of 160 MHz meeting all timing constraints to drive the hybrid DPWM. The tapped delay line in closed-chain mode resembles a ring-oscillator. The open-chain tapped delay line configuration which is used in this proposal relaxes some of the necessary conditions for ring-oscillator to perform and hence the design becomes simple. Limited fine resolution of hybrid DPWM at a high switching frequency has been addressed by an edge-triggered hybrid DPWM. This effectively overcomes the maximum achievable switching frequency barrier due to hardware timing constraints and improves the linearity of hybrid DPWM. The proposed dual mode operation of hybrid DPWM design has been verified for an 8-bit hybrid DPWM in 0.5 μm CMOS technology and has also been verified on an experimental Altera DE2 FPGA setup. The average current consumption of dual mode hybrid DPWM is 2.5 mA at 3.3 V in 0.5 μm CMOS technology. Average power consumption of the dual mode dual switching frequency hybrid DPWM is 8.415 mWatt, while periodically switching between dual modes and providing the corresponding control signals of 1.56 MHz and 25 MHz. Single mode operation of an 8-bit hybrid DPWM consumes 12.48

mWatt while providing 1.56 MHz switching frequency. The dual mode 8-bit hybrid DPWM consumes 32.57% less power compared to an 8-bit normal hybrid DPWM. The active chip area of DPWM is 0.07 mm^2 in 0.5 μm CMOS technology. This proposal achieves a 160 MHz switching frequency with 4-bit resolution during transients and provides 10 MHz switching frequency with 8-bit resolution at steady state on an Altera DE2 FPGA experimental setup. The dual mode hybrid DPWM also provides instantaneous overcurrent protection feature for voltage controlled DC-DC converter. Thus the performance of hybrid DPWM has been enhanced, though ADC and compensator performance remains unaffected in the complete digital controller.

Each module of the digital controller has been designed based on HDL verilog code. Synopsis synthesis (Design Analyzer), timing verification (Prime Time), chip layout (Astro), and post layout chip simulation (Nanosim) tools have been used to implement the complete digital controller chip design in 0.5 μm CMOS technology.

A synchronous buck converter of switching frequency 1 MHz has been fabricated for the complete closed loop experimental prototype. Discrete components have been used for constructing the delay line based ADCs. A folding logic, error detection block, binary encoder, dual mode error control, look up table based programmable digital compensator and an 8-bit edge-triggered hybrid DPWM design have been implemented on the Altera DE2 cyclone II FPGA.

Different performance metrics are considered to evaluate different digital controller proposals: *transition time*, *settling time*, *switching frequency*, *regulated voltage range*, *converter efficiency*, *on chip silicon area* and *power consumption*. Different experiments have been conducted to study the robustness of proposals such as impact of load change, reference voltage change and target frequency change.

With the integration of the proposed digital controller architectures, truly adaptive, voltage mode regulation loops have been realized for DVS.

Keywords: DC-DC converter, Digital Controller, Power Management, Dynamic Voltage Scaling (DVS), Wide dynamic range, Analog-to-Digital Converter (ADC), Delay Line, Piecewise-linear, Multiple Overlapped band, Resolution, Switching frequency, Dual mode, Digital PID compensator, Look-up Table (LUT), Edge-triggered, Digital Pulse Width Modulator (DPWM).