

Abstract

Accurate estimation of timing and power characteristics of a circuit is a fundamental component of the digital circuit design validation process. Correctly estimating the critical delay of a circuit is necessary for determining the speed of operation of the circuit. With the steady rise in chip density, excessive power dissipation is now a burning problem for the VLSI design community and accurate estimates of the power consumption of a circuit are needed for determining the thermal and electrical limits of a design.

We have proposed an integrated framework for both timing and dynamic power estimation that uses the event propagation model to realistically represent the internal events in a circuit. The timing delays within a circuit are accurately traced by tracking the events traveling from the inputs to the outputs. Events are also the primary cause of the dynamic power consumption of a circuit.

The complexity of the event propagation model is high owing to the 2-vector requirement. Thus, a powerful computational framework is needed which makes it possible to handle large circuits without compromising on the accuracy and efficiency of the process. In recent years, SAT based modeling of difficult problems in design of digital circuits has emerged with attractive possibilities and SAT based techniques have proved to be better at scaling to larger circuits than traditional algorithmic methods.

In this thesis, we propose a SAT based modeling of event propagation within a circuit in operation. This detailed model provides an integrated framework for accurately estimating both the timing delay and the dynamic power consumption of a circuit. The proposed methodology scales well to large circuits without sacrificing on accuracy, even with industry standard gate delays of 0.01ns precision. We experiment with a wide range of gate delay models starting with the simplest fixed gate delay model and going on to richer but also more complex delay models like the pin-to-pin delay model, the rise/fall delay model, the inertial delay model and the bounded delay model.