ABSTRACT

Customization of test patterns is an integral part of VLSI testing process. Patterns generated by test generation tools and algorithms leave a good number of input bits as don't cares (unspecified). Their values can be filled by the test engineer to facilitate the testing process. Though, traditionally the don't care bits are exploited to achieve compaction, these have also been used for test power reduction. This thesis aims to find the utility of the don't care filling policies to generate customized test sets for different objectives. First, a don't care filling strategy has been designed to get a trade-off between controlling dynamic and leakage power consumption of the circuit-under-test (CUT), while most of the existing approaches minimize dynamic power alone. Next, the strategy has been extended to thermal aware testing. In this approach, the don't cares have been filled up, such that, both peak temperature of the chip and the temperature variance across the chip get reduced. To reduce test cost, often only a subset of patterns are applied in a test session, giving rise to a trade-off between test time and the confidence in the correctness of the CUT. The next work proposes such a strategy which gets augmented by the don't care filling technique proposed in the thesis. When a chip fails manufacturing test, diagnosis is the process to predict the probable fault locations, to be finally checked using electron microscope. While a test set used in production test is optimized to cover more number of faults, diagnostic test set should have the ability to distinguish between faults. The don't care filling strategy has also been extended in this thesis to customize the test set for diagnostic purpose.

KEY WORDS: Test data compression, Don't care fill, Test power reduction, Peak temperature, Thermal variance, Thermal aware testing, Particle Swarm Optimization, Confidence aware testing, Weighted Switching Activity, Fault Diagnosis, Distinguishablity Metric.