Abstract

The computational workloads of everyday applications have increased manifold due to rapid technological advances in recent times. As a result, today's computing devices have become increasingly power-hungry. Approximate computing is an emerging solution for developing low-power designs targeted toward error-tolerant applications with inherent resiliency properties. Several approximate adders and multipliers have been proposed targeted for energy-efficient system design specific to error-tolerant applications. Error metrics such as mean error distance (MED), mean square error distance (MSED), and worst case error (WCE) have been used widely in existing studies to characterize and compare various approximate adders. This thesis proposes three independent algorithms to compute the exact values of MED, MSED, and WCE, respectively, for an Approximate Least Signifiant Bit (LSB) Adder (ALA). The algorithms are based on an iterative computation of intermediate parameters from the least significant sub-adder block to the most significant sub-adder block. The simulation results show that for 16-bit ALAs, the computational run-time of the proposed MED, MSED, and WCE algorithm is much faster than the traditional Monte Carlo (MC) simulations. In this thesis, we have introduced two variants of a broken array approximate Booth multiplier design called SIBAM (Sign-Inclusive Broken Array Booth Multiplier) with partial error correction through discarded sign bit addition. The addition of the sign bits drastically improves the error performance of the broken booth multiplier while incurring minor area and power overhead. Since the accuracy requirements of an application can vary dynamically at run-time, there is a justified need to design reconfigurable approximate circuits with varying power requirements proportional to computational accuracy. This thesis also proposes a novel accuracy reconfigurable approximate booth multiplier circuit called ACBAM (Accuracy Configurable Broken Array Multiplier), which is based on the SIBAM design. The horizontal and vertical breaks introduced in the booth multiplier circuit are controlled using external control signals stored in a ROM. The proposed reconfigurable multiplier achieves more significant power savings than accurate multiplier circuits and state-of-the-art configurable multiplier designs.

Keywords: Approximate Computing; Error-Tolerant Applications; Approximate LSB Adder; Mean Error Distance; Mean Relative Error Distance; Approximate Adders; Booth Multiplier; Accuracy Configurable Multipliers.