Abstract

Network-on-Chip is seen as a solution for addressing the limitation of the bus-based communication in Multiprocessor System-on-Chip (MPSoC) based embedded system design. An important design challenge in such systems is the application mapping problem. In the systems designed for executing real-time services, in addition to the correctness of functionalities, timeliness becomes an important factor. Violation of timing requirements can result in performance degradation or even system failure causing severe consequences to human life. In addition to task mapping techniques considering real-time constraints, priority ordering of flows is as important as the mapping itself, when the interference patterns are considered.

In the thesis, NoC design space has been explored with both static and dynamic application mapping techniques. The work also addresses the priority assignment problem, in case of static and dynamic mapping. A Heuristic Driven Genetic Algorithm (HDGA) has been developed for priority assignment problems. It has been further extended by proposing a unified technique for simultaneous optimization of task mapping and priority assignment (eHDGA). eHDGA algorithm has been validated on two real time industrial applications of autonomous vehicle and avionics computer. The research work has addressed the dynamic mapping using Deadline and Energy-Aware dynamic task Mapping and Scheduling (DEAMS) algorithm with priority assignment by graph based approach. In addition to the topological mapping of tasks on the cores and priority of communication flows, the communication flow latency and schedulability also depends on the flow routes. Most studies on wormhole-switched priority preemptive NoC assume deterministic XY routing. The research work explores the effects of having non-deterministic minimal routing on schedulability. Another work deals with mapping of applications from a security perspective. It finds out possible convex shapes (rectangle or square) of mapping for each application and places the mapped shapes of different applications dynamically on a NoC fabric to prevent side channels by ensuring spatial isolation.

Keywords: Network-on-Chip; Real-Time systems; Flow priority assignment; Genetic Algorithm; Task Mapping; Schedulability; Worst-case Latency; Worst-case schedulability analysis; Heuristic driven; Static Application Mapping; Dynamic Application Mapping; Minimal routing; Particle Swarm Optimisation, Security critical Mapping; mission and safety critical applications; avionics; automotive.