Abstract

This thesis has mainly focused on developing low complexity and efficient VLSI architectures for Low Density Parity Check (LDPC) codes. LDPC codes constitute a class of linear block codes, which were first introduced by Gallager, achieve error performance of a fraction of a decibel away from the Shannon limit under Sum Product Algorithm (SPA) decoding. From the recent literature, it can be seen that the hard decision decoding algorithms are an attractive research topic due to their low complexity and fast computation. In the next generation of communication systems, throughput and power consumption are the key challenges. LDPC error correction modules are a part of the system and so, their design needs to be optimized to attain high throughput of the overall system. Compressed Sensing for signal specific applications has gained interest in recent times. A special class of signals called binary sparse signals have come into existence in many practical applications. In the first part of the thesis, a fully parallel VLSI architecture for Multi Threshold Bit Flipping (MTBF) algorithm has been proposed. The algorithm is modified to make it more amenable to be implemented in hardware. The proposed architectures demonstrate high throughput comparable with that of the state-of-the-art decoder designs, which paves the way for implementation of Finite Geometry LDPC (FG-LDPC) codes with low complexity. Next, VLSI architecture of Interval Passing Algorithm (IPA) for Binary Compressed Sensing (BCS) is proposed using binary LDPC matrices based on Finite Geometry. The IPA is modified so as to reduce its complexity without compromising the performance. Moreover, VLSI architecture of the modified algorithm is proposed. The proposed architectures demonstrate high frequency of operation and low reconstruction time. Although binary LDPC codes approach the channel capacity theoretically, they should be designed to have very long codeword length in order to do so. Non-binary (NB) LDPC codes defined over Galois Field GF(q), where q>2, provide better error performance while compared to their binary counterparts for moderate code length, albeit with a significant increase in the decoding complexity. In this work, a memory efficient architecture, which uses a central memory structure called Multiport RAM (MPRAM) that is built using Block RAMs (BRAMs) for Iterative Soft Reliability Based (ISRB) algorithm, has been proposed. The proposed work provides a user programmable decoder with variable parity check matrix.

Keywords: Low Density Parity Check (LDPC) Codes, Binary Compressed Sensing, Low Complexity VLSI Architecture, Bit flipping Decoder, Non-Binary LDPC.