Abstract

With the advancement in fabrication technology, multiple digital cores are getting integrated on a single die, leading to multiprocessor system-on-chip (MPSoCs). Data sharing among the digital cores in the MPSoCs through Networks-on-chip (NoC) are becoming popular as it provides scalability, flexibility and high throughput. The performance of NoC is highly dependent on the characteristic of the global interconnects realizing the NoC. As the global interconnects are lossy links, it is a challenge to transmit high speed data efficiently across them. For energy efficient high speed data communication, full swing signaling across the segmented interconnects with repeaters is getting replaced by low swing signaling across repeaterless single interconnect.

In this thesis, we have proposed a number of energy efficient transceivers for high speed data communication across the repeaterless on-chip interconnect. All these transceivers are meant for current-mode signaling scheme which is known to be a power efficient signaling scheme. A common feature of these transceivers is that the input impedance of the receiver is sufficiently low which helps to eliminate the necessity of passive terminator and thereby, reducing the overall power dissipation without sacrificing the data rate of the link. Firstly, a current-mode transceiver has been proposed suitable for bi-directional half-duplex link. The proposed transceiver can either be set as a transmitter or receiver. Secondly, a new transceiver architecture has been proposed for simultaneously transmitting and receiving data over the same interconnect i.e. for full-duplex link. The transceiver has a special directional inverter buffer circuit to achieve full duplex signaling. This improves the energy efficiency of the link by a factor of ten. Thirdly, an energy efficient current-mode tri-line transceiver has been proposed for coded differential signaling. Compared to an existing technique using resistive terminated receiver, it has 2.4 times better power efficiency. An encoding scheme compatible with the proposed transceiver has also been proposed to enhance the wire efficiency further. And lastly, we propose to use a hybrid architecture suitable for multipoint-to-multipoint signaling which uses both voltage mode and current-mode receivers to enhance the overall efficiency. In addition, an energy efficient hybrid transceiver suitable for this hybrid architecture has been proposed.

These transceivers have been designed in 0.18 μm, 1.8 V CMOS UMC process. Except the first one, all the proposed transceiver circuits along with their respective interconnects have been fabricated for the validation of the concepts. Measured results of the implemented prototype have been provided in this thesis.

Keywords- On-chip interconnect, global interconnect, high speed link, serial communication, network-on-chip, current-mode, bidirectional, full-duplex, coded differential.