Abstract

Video segmentation is crucial and indispensable task in many video processing applications. It is also becoming more challenging as the frame resolution and frame rates are increasing rapidly. Speed of conventional processors is saturating and parallel processing with dedicated hardware is the need of the hour for video processing. In this thesis, a generalized parallel processing framework based on cell network is used to accelerate video segmentation task. High speed video segmentation is achieved in two ways. First, few of the sequential classical spatial segmentation algorithms are transformed into local operation based pixel grid parallel algorithms. Second, these algorithms are mapped onto cell network based parallel architectures implemented using structural VLSI design in FPGA. The cells or processing elements act as oscillators in Locally Excitatory Globally Inhibitory Oscillator Network (LEGION) and digitally encoded by Finite State Machines (FSM). The chosen representative segmentation algorithms are region split and merge, region grow, watershed algorithm, edge based segmentation and graph cut based segmentation. In region split and merge, a parallel local rule based segmentation algorithm and multi-tier cell network architecture is proposed to achieve sub millisecond processing time for live PAL video segmentation. In region growing segmentation scheme, real time full field of view PAL video segmentation is achieved by employing cell networks based on semi parallel seeded region growing and fully parallel minimum maximum predicate based novel algorithm. In next chapter, a novel parallel hill climbing based watershed segmentation algorithm is proposed and a LEGION based cell network architecture is designed to perform watershed segmentation in parallel manner. In edge based segmentation, a novel coupled oscillator based edge detection algorithm and cell network based architecture is introduced to detect edges in video sequences. A pipelined architecture is proposed with throughput of 125 HD frames /second. Finally, one of the state of the art algorithms, graph cut segmentation algorithm is targeted for parallel implementation. A novel parallel algorithm called ‘Successive Flow’ for finding maximum flow in graphical network is introduced and implemented in a LEGION based parallel architecture to cut segment of

video frames into background and foreground objects in real time. As the parallel cell network consumes very large hardware resource in FPGAs, few of the proposed algorithms are converted into systolic architecture to compare the performance in terms of speed and area.

Keywords: Cell Network, Video Object Segmentation, Parallel Algorithms, LEGION, VLSI Architecture, FPGA