Abstract

A conventional sensor signal acquisition system architecture includes separate signal conditioning section followed by ADC section and hence, consists of a long chain of successive circuit blocks with each performing separate functions. Each of the constituent circuit blocks require significant amount of power and implementation area. In contrast, the present research puts forward an integrated second-order hybrid delta-sigma modulator ($\Delta\Sigma$M) based compact signal acquisition system architecture. In the proposed system, a differential difference amplifier (DDA) has been customized for dual purpose roles, namely as instrumentation amplifier and as an integrator of $\Delta\Sigma$M. Implementation of all functionalities of signal acquisition system, like balanced high input impedance and programmable amplification for the input signal from the sensor, filtering of signal to remove high frequency noise components, anti-alias filtering, and digitization have been incorporated within this $\Delta\Sigma$M based compact acquisition system. Further, an intentional difference between the transconductances of the input pairs of the DDA has been proposed to reduce the effect of input resistor thermal noise of the front-end R-C integrator of the $\Delta\Sigma$M. Additionally, chopping modulation has been utilized in order to minimize the effect of flicker noise. Thus, the proposed architecture is an aggregation of the entire signal acquisition system functions within a single block which is the $\Delta\Sigma$M. Consequently, it is a compact precision readout front-end that is size, cost and power efficient.

Using the proposed system architecture, a prototype low-to-medium frequency signal readout front-end system has been implemented in CMOS 0.18-μm technology. The functioning of the system and its constituent blocks have been verified through extensive simulations in Cadence Virtuoso and MATLAB Simulink platforms. The

system has been designed to yield a peak SNR of about 80dB (hence, a resolution of 13 bits) and dynamic range of about 109dBFS for an input signal band of around 1kHz, while consuming less than 100μW of power. Physical design of the proposed front-end has also been carried out, and detailed post-layout simulations have been performed for confirming the performance of the designed layout with the circuit schematic simulation results. Thereafter, the design has been fabricated in SCL's 0.18-μm CMOS process and the resulting test-chip has been characterized. The measured (and post-layout simulated) performance of the designed system has then been compared with that of reported similar ΔΣMs. The relatively low-frequency design presented here is for demonstrating the efficacy of the proposed topology. However, it may be noted that the same signal acquisition system architecture can be used for higher operational frequencies as well.

Keywords: Analog front-end, analog to digital conversion, ADC, delta-sigma modulator, instrumentation amplifier, sensor interface, sigma-delta, signal acquisition, signal conditioning.