Abstract

This research work primarily deals with the COordinate Rotation DIgital Computer (CORDIC)-based conventional and modulated Sliding DFT (SDFT) architectures for computing a few selected bins within the whole spectrum. The SDFT updates the frequency spectrum whenever a new sample arrives at the input in real-time and is computationally more efficient compared to the fast Fourier transform (FFT). In the real-time scenario, the problem of spectral leakage is unavoidable and is therefore necessary to apply windows while computing the DFT to minimize leakage. We have proposed the SDFT architecture integrated with the triangular window, which is relatively easier to implement, and with the Hann window for relatively better performance. The proposed triangular windowed SDFT architecture is modified to provide the accurate outputs based on the exact transfer function with a high-throughput rate compared to the existing designs. Further, we have developed two algorithms for the Hann windowed SDFT architectures, which can also be extended to high order generalized cosine windows. An error containment feature (or refreshing mechanism) is included in the proposed SDFT architectures to limit the error-accumulation compared to the existing designs, where the error is unbounded due to its recursive nature. All the proposed SDFT architectures are scalable with the transform length and the supported number of calculable bins. The computational accuracy of the proposed SDFT architectures in terms of the angle-approximation error and the worst-case truncation error is also presented. We have proposed a dual-memory based architecture for the reconfigurable 128- to 2048-point FFT processor based on the decimation-in-frequency (DIF) algorithm to compute the complete spectrum for non-overlapping windows in real-time. The memory-based FFT architecture has been proposed with a single radix-2 processing element (PE), and also with multiple parallel radix-2 PEs for achieving higher throughput. We have developed a novel conflict-free memory addressing scheme for the proposed reconfigurable FFT architecture to meet the specifications of the orthogonal frequency division multiplexing (OFDM)-based communication systems. All the proposed designs have been synthesized on both FPGA and ASIC platforms.

Index Terms: CORDIC, DFT, FFT, sliding DFT (SDFT), modulated SDFT (mSDFT), spectral leakage, windowing, real-time spectral analysis.