Abstract

Network-on-Chip (NoC) provides a communication backbone for on-chip packet transmission between different Intellectual Property (IP) blocks in system chips. The NoC paradigm helps to overcome the drawbacks of bus-based System-on-Chip (SoC) by providing a more flexible, scalable and effective communication platform. With rapid advancement in deep sub-micron technology, another issue that comes into consideration is the system reliability. As more number of transistors are packed onto a single chip, the probability of their failure also increases. From the aspect of Network-on-Chip fabric, faults may damage links, routers or both. To handle such faults, different strategies have been employed in this thesis, which include modification of router architecture, network reconfiguration and use of spare routers and links. These strategies have helped to tolerate network faults along with improvement in system reliability. It may be noted that the failure rate of a chip varies with its working temperature. A temperature dependent reliability model has been developed for proper evaluation of the system reliability. The model has been used for a reliability-aware mapping algorithm, developed for mapping tasks onto mesh based NoC. The approach attempts to maximize system reliability with a constraint on average packet delay (APD). A Particle swarm optimization (PSO) based formulation and a Mixed Integer Linear Programming (MILP) have been used. The proposed approaches have improved system reliability and network performance. A fault tolerant NoC design also involves mitigation of processor faults. Faults in processors are divided into two parts- transient and permanent faults. A task executing on a processor affected by transient fault gets corrupted. On the other hand, in case of permanent faults the processor becomes defunct. To overcome such situations, different fault tolerant strategies have been used. For transient faults, checkpointing, task re-execution and replication have been used. In case of permanent faults, active and passive replication of tasks have been used. To mitigate the effect of these faults in real-time embedded systems, consisting of NoC based multi-processors, fault tolerant dynamic mapping and scheduling algorithms have been proposed.