Chapter 1

Introduction

Power Supply and power management units are the most fundamental and indispensable components found in any integrated circuit (IC). The supply voltage needs to be stable, constant and accurate to ensure proper operation of the analog, digital and mixed signal circuits in the IC. Such stable voltages are obtained from the power management unit which is powered from the main input supply like a battery or an $AC - DC$ regulator. The power management circuit does the job of conversion of the input voltage level to the desired level and also maintains its output level independent of the load current and input fluctuations. There is a constant endeavor to build a highly power efficient converter with small size and low weight. Low voltage power converters are indispensable to develop hand held devices [1]. With the progress of technology the required internal supply voltage is continuously decreasing. This is mainly to reduce the dynamic power loss of a system in quadratic manner (CV_{dd}^2) [2]. In these portable systems, DC-DC voltage conversion is required to generate different voltage levels from a single external battery source. So the DC-DC converter is actually intermediate module of the battery and the core circuits. The core circuits are treated as load for the converter. High efficiency conversion helps to increase the life time of the battery. Based on the basic requirement of DC-DC voltage conversions, there are basically two classes of converters. One class is used for stepping up the voltage level and the other class of converter is for stepping down the input supply voltage. The DC-DC converter which does the step-down job is popularly known as 'Buck Converter' while the other one is widely called as 'Boost Converter'. Based on implementation there are three major categories of step-down DC-DC converters; viz., inductor based, switched capacitor based and linear regulator. This research work is on switched capacitor based buck converter integrated with a linear regulation loop.

1.1 Literature Survey

The development of the monolithic regulators started in the late nineteen sixty [3]. There after a considerable effort has been made for the improvement of their performance metrics viz., power efficiency, output voltage ripple, supply and load regulations etc. There are three major categories of step-down DC-DC converters, viz. Inductor based, switched capacitor based and linear regulator are available. A brief survey on the research work in each filed are depicted in the next few sections.

1.1.1 Inductor Based DC-DC Converter

Inductor based converter is the first choice to make a highly efficient buck converter. The basic schematic of inductor based buck converter [4], [5] is shown in Fig. 1.1. There are two complimentary switches, S1 and S2 which are turn on and off depending on the input pulse given to the switches. The inductor L and capacitor C_L basically form a low pass filter. The input supply voltage, V_{in} is chopped by S1 and S2 and produces a rectangular voltage having average level of the defined output voltage. The low pass filter passes the d.c. voltage to the load. The duty cycle of the rectangular input pulse to the switches actually determines the average output level. There may be several arrangements of switches and filter components to produce different output voltages which may be lower or higher and same or opposite in polarity with respect to the input supply voltage.

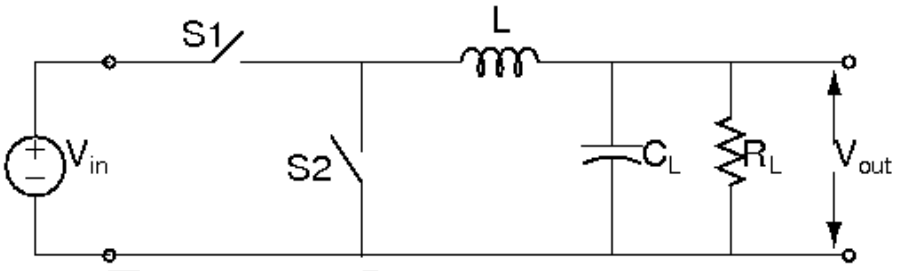

Figure 1.1: Basic Schematic of Inductor Based Buck Converter

For achieving more than 95% of power efficiency at heavy load (i.e., maximum load current) and light load (i.e., minimum load current) condition, different control schemes viz., Pulse width modulation (PWM) and Pulse Frequency modulation (PFM) are used, respectively. It is observed that PWM is usually advantageous in terms of good regulation and power efficiency when the converter is in heavy load of operation. On the other hand, using PFM technique is beneficial in light load of operation [6]. In this context, a

point to be added that the different parameter sensing techniques in the different mode of control are evolved. Hassan Pooya et al. had reviewed six available current sensing techniques. They also introduced a new scheme to measure the current more accurately [7]. Cheung Fai Lee and Phili Mok had introduced a monolithic current-mode CMOS DC-DC Converter with integrated power switches and a new on-chip current sensing technique for feedback control. The sensed inductor current which is combined with the internal ramp signal can be used for current-mode DC-DC converter feedback control with the help of proposed scheme. In addition, the authors had implemented the scheme without any extra Input / Output (I/O) pin for current mode controller [8]. Cheng- Hui Chang et al. had achieved 98.2% accuracy of current-sensing is while the core circuit power loss is within 90 mW [9].

The research in multiphase voltage regulator module (VRM) to provide load current with higher rating is also progressing. Abram P. Dancy et al. had designed a high efficiency multiple output DC-DC converter where the key features of that design are its low-power dissipation, reconfigurability [10]. Angel V. Peterchev et al. had developed PWM architecture in multi phase voltage regulation module (VRM) [11]. The power losses which are incurred by the different ways at the time of operation of the buck Converter are modeled by different research groups [12]. Different techniques have been mathematically formulated and implemented to minimize those losses. Volkan Kursun et al. proposed low voltage swing MOSFET technique to enhance the power efficiency of high frequency switching DC-DC converter [13].

However, the main disadvantage of the buck Converter is the presence of their off-chip inductors. It makes the converter bulky and noisy. An effort is given to bring the inductor within the chip [14] but low Quality factor (Q) value of the inductor limits it on-chip implementation. There are some techniques to reduce the electromagnetic interference (EMI) of the inductor [15].Eduard Alarcon et al. had designed a three level buck Converter [16]. It offers reduced size of magnetic components, fewer amounts of switching ripple and switching losses in comparison to any standard or two levels buck Converter but still the size of the inductor is high which restricts to embed the entire module within the chip.

On the other hand, on-chip, inductor-less, power-efficient DC-DC converter with low output voltage ripple applicable for the analog-embedded applications are in high demand particularly in battery operated compact system. Further miniaturization of the converter is a challenging research topic to embed the converter within its application chip. The obvious advantages of such embedded converters are size, weight and EMI.

1.1.2 Linear Regulator

Another option of on-chip voltage conversion is through linear regulator with zero output voltage ripple and capability of on chip implementation. The basic schematic of linear regulator is depicted in Fig. 1.2. It is made of an error amplifier followed by a pass transistor. A fast dynamic response is also be provided by this regulator [17]. These features make linear regulator suitable for analog and embedded application. Gerrit W. den Besten and Bram Nauta developed a 5 V to 3.3 V linear regulator which can supply more than 200 mA of current while the output within a margin of 10% of its nominal value [18].There was an attempt by Mohammad Mahdi Ahmadi et al. to develop a linear regulator in 0.18 μm CMOS process [19].

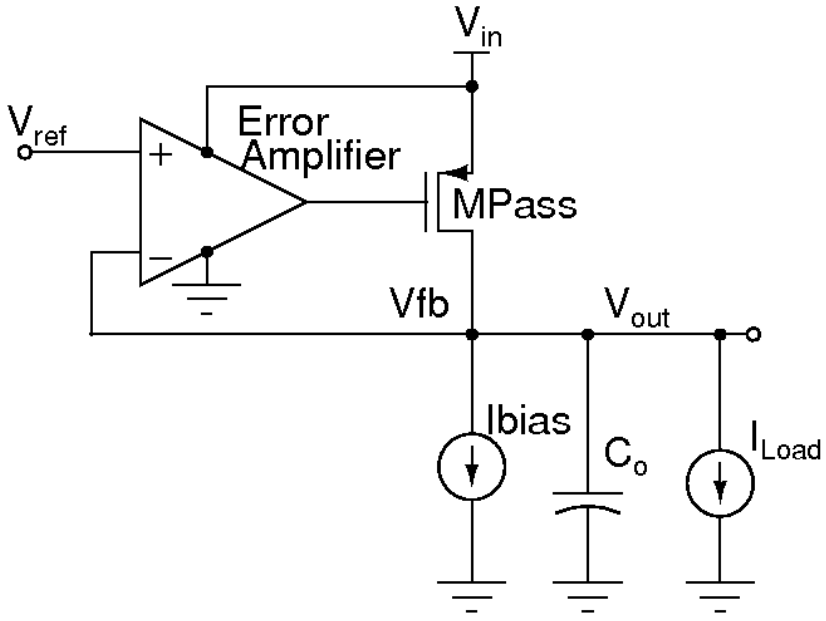

Figure 1.2: Basic Schematic of Linear Regulator

The power efficiency is high for a low dropout (LDO) regulator where the difference between an input and the corresponding output voltage is very less. Tetsuo Endoh et al. had used a flexible control technique to improve the current efficiency of the linear regulator and there by improving power efficiency at light load condition [20].
Frequency compensation strategy for an error amplifier of particular type of linear regulator is also a challenging task. Ka Nang Leung et al. had developed a capacitor free CMOS LDO for system on chip application to reduce the board space and number of pin

counts [21]. A robust frequency compensation strategy is demonstrated by Chaitanya K. Chava et al. where the authors generated a zero internally rather than depending on the zero developed by the load capacitor [22]. Xiaohua Fan et al. had also contributed in the compensation of LDO with a motivation for research on high-gain wide-bandwidth amplifiers driving large capacitive loads [23].
However, its power efficiency reduces linearly with the increase of input and output voltage difference. This becomes a major concern for battery operated system, where, battery voltage remains same while the required internal voltage reduces with progress of IC fabrication technology.

1.1.3 Switched Capacitor Based DC-DC Converter

Looking into the need of embedded power management unit, a new area of switch capacitor based converters is emerged for overcoming the drawbacks of inductor based converters [24], [25]. These type of converter topologies are meaningful to improve the efficiency. Here, the basic idea is to use switches and capacitors for controlling the energy transfer. Monolithic integration is also possible through it. The basic schematic of the switched capacitor based buck converter and the corresponding phases of the control signals are shown in Fig. 1.3 and Fig. 1.4. It posses the advantage of reduced size and weight.

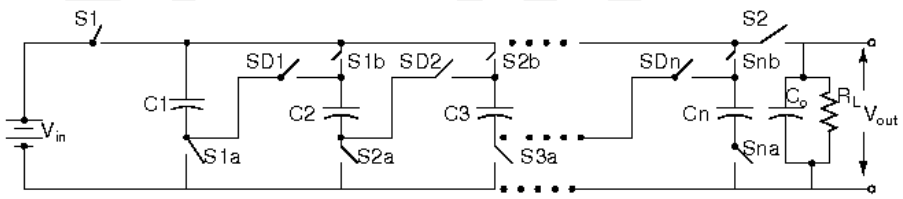

Figure 1.3: Basic Schematic of Switched Capacitor Based Buck Converter [28]

However, small size of capacitors may leads to a considerable amount of switching noise which restricts its analog application. The switching noise can be reduced by using large capacitor(s) (may be of the order of μF) [26] but it may not be possible to implement these within a chip. Moreover, embedded switched capacitor based converters have low current driving capability. Although the approach proposed by Jifeng Han et al. has not been implemented for embedded DC-DC converter, but it was a new technique to reduce the output ripple in switch capacitor based DC-DC converters [27]. It uses a new method called as Interleaved Discharging (ID) to reduce ripple and improve power efficiency.
There is a recent trend of combining a switching regulator (inductor based or capacitor

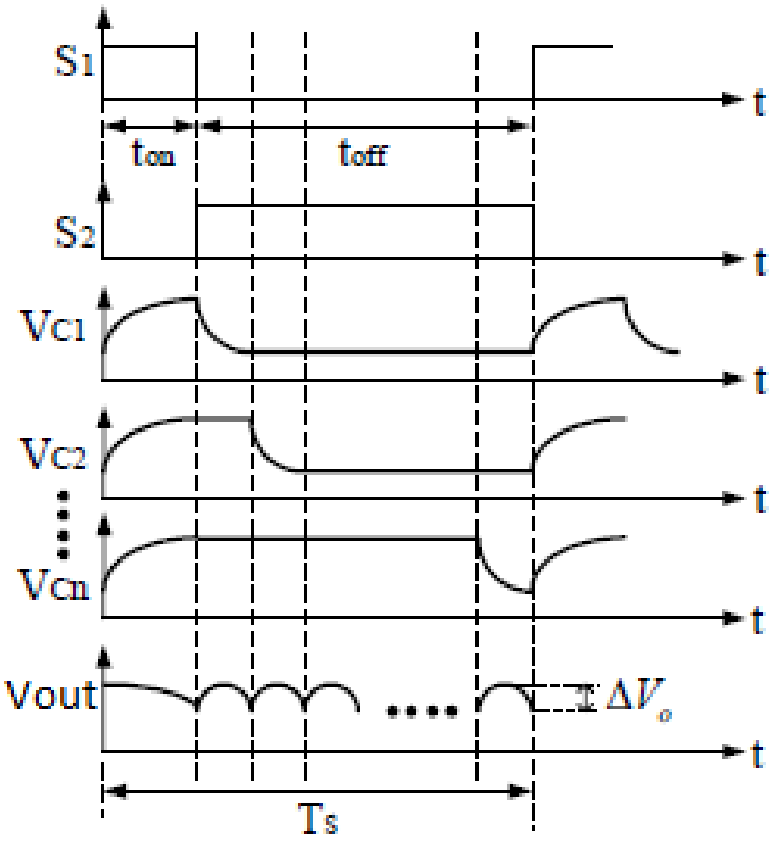

Figure 1.4: Phases of the Control Signals of the above Switched Capacitor Converter [28]

based) with a linear regulator to achieve good power efficiency with low output ripple. For instance, combining a switched capacitor converter and a linear regulator gives a high dropout converter with good power efficiency. In these hybrid converters the output ripple is kept low by using external capacitor. The linear regulator in the hybrid converter also helps to achieve better load and line regulation. A pre-specified regulated output voltage level may be achieved by it. There is a steady development on the research of embedded hybrid DC-DC converters. A brief overview of this development is given below:

George Patounakis et al. had designed and implemented a hybrid DC-DC converter which is a combination of switch-capacitor converter and a linear regulator [30], suitable for high dropout converter with good power efficiency. In this hybrid converter the output ripple is high as the flying and load capacitors are on-chip implementable range but the authors did not concentrate on the ripple reduction issue.

There is a hybrid converter topology which can be implemented on-chip without any external capacitor and its output ripple is maintained within acceptable level [33].
In case of embedded switched capacitor based DC-DC converters during switching transition a short circuit path from output to ground and Vdd to ground is created due to the use of overlapping clocks. This eventually degrades the power efficiency of the converter in the form of shoot-through current. This shoot-through current can be reduced by using non-overlapped clocks such as break before make mechanism [41], [34]. However, in embedded applications where the load capacitor is very small, non-overlapped clocks results in dip in the output voltage due to temporary shortage of charge at the output. The dip can be reduced by using an extra transistor to compensate this momentary deficiency of charge at the cost of reduction in power efficiency [34].
In addition to shoot-through current the short circuit paths also creates 'dip' at output voltage. This is more prominent in case of on-chip DC-DC converters for embedded applications, where the load capacitance is very small (pF range). It may be shown that for a given capacitance the ripple voltage increases with the increase of output current. This ripple can be reduced by increasing the clock frequency of the converter. However, this increases the switching loss and shoot-through currents and degrades the power efficiency.
Time-interleaving switching scheme for switching converters [47] was proposed to reduce output voltage ripple. The same scheme is utilized in the dual switched capacitor converter to achieve smaller output voltage ripple.
In case of time interleaving converter with $2N$ number of elements, the N elements are in charging phase and remaining are in charge-recycling phase and each element is driven by one of the $2N$ clock-phases. At each switching transition one pair of flying capacitors change their phases while all the other remain in their respective phases.
For the same output current the dual switched capacitor converters output voltage ripple is reduced by N times. In addition, as the size of each switching transistor is decreased by N times, the shoot-through current at each transition decreases by N times. This reduction in shoot-through current reduces the dip at the output, thus further reduction in ripple. In time-interleaving converter, though the switching and shoot-through current losses at each transition are scaled down by N, the total loss per clock period remains same due to $2N$ transitions per clock. Though the time interleaving scheme reduces the output voltage ripple, it suffers from shoot-through current loss during switching transitions.
To solve the shoot-through current problem mentioned above, a non-overlapped rotational time interleaving (NRTI) scheme is evolved [48]. In this the shoot-through current is eliminated by avoiding direct transition of flying capacitor from charging phase to charge recy-

cling phase and vice verse. As shoot-through current is eliminated in the NRTI converter, supply current variation is also negligible. This unique feature of the converter eliminates possible ground bounce effect of the converter. NRTI scheme can also be applied to the step down converters where the output is fraction of $2/3^{rd}$, $1/3^{rd}$ and $1/2$ of supply voltage [58].

It is to be noted that the output voltage of a switched capacitor network is a fraction of its input voltage and the fraction is a function of load current and switching frequency. Thus, a closed loop control is essential for regulation. So, current and voltage regulation are used. NRTI switched capacitor DC-DC converter is cascaded with a linear regulator to get the output voltage at a pre-specified level with a wide dynamic range of load current and supply voltage. In other words, hybridization with linear regulator provides a better line and load regulation [52].

However, the Switched capacitor architecture in [48] has only Vdd/2 option. Therefore, it suffers from power efficiency degradation particularly for a very low dropout application. On the other hand in [55], [54] same flying capacitors are used to provide three different step down fractions of its input supply (Vdd) to meet the different technology nodes. This re-utilization property of the same capacitor helps to improve the area overhead of the converter.

1.2 Motivation and Objective

From the above discussion the motivation of this dissertation is to develop building blocks of the power management module. So, the objective of this work is to design and implementation of a switched capacitor based DC-DC converter which is the heart of any power management module with better performance like reduced output voltage ripple, improved power efficiency and increased area efficiency. It is known that the output voltage ripple is alarmingly high in an embedded converter as its flying and load capacitors are within on-chip implantable range (within 1 nF). Although the ripple can be reduced with the increase of switching frequency but the switching loss increases and hence, the power efficiency reduces. So, evolution of technique for reduction of output voltage ripple of switched capacitor based converter particularly for embedded application is needed.

As mentioned before in existing switched capacitor converters during switching transition a short circuit path from output to ground and supply (Vdd) to ground is created due to the use of overlapping clock signals. This degrades the power efficiency of the converter

in the form of shoot-through current. This shoot-through current can be reduced by using non-overlapped switching phases of the capacitors. However, in embedded applications the use of non-overlapped control phases results in output voltage dip at every phase transition due to temporary shortage of charge at the output.
Recently, work on reconfigurable architecture is getting introduced where the same switched capacitor module is reconfigured to generate different step-down voltage and hence, the area efficiency of the converter increases. However, each configuration has limited load driving capability. It is observed that the driving limit can be increased by using a regulation loop and dynamically reconfiguring the architecture. Motivated by the shortcomings of the existing embedded DC-DC converters the present dissertation aims at proposing research topologies starting from ripple reduction techniques of a dual switched capacitor based converter and finally advancement towards the development of a reconfigurable embedded DC-DC converter with high current driving capability, low output ripple and improved power efficiency. The work done of the dissertation is summarized by the following points:

- Study the available literature on DC-DC converters mostly on-chip and embedded implementation and figure out the shortcomings of the existing topology.
- Propose techniques to reduce the output voltage ripple of an embedded dual switched capacitor based DC-DC converter. Analysis and simulation of the proposed techniques to validate the research idea.
- Design and layout of the dual switched capacitor based hybrid DC-DC converter by incorporating the above mentioned ripple reduction techniques.
- Testing and measurement of the fabricated test chip.
- Introduce a switching scheme, called NRTI to reduce the ripple within acceptance level and elimination of the shoot through current loss which improve the power efficiency. Design of generation different step-down fractions of input supply voltage using NRTI scheme.
- Design and Simulation of the dynamically reconfigurable NRTI switched capacitor converter to demonstrate the improvement of its performances.

The contributions and organization of the Dissertation are given in the next section.

1.3 Contributions and Organization of the Dissertation

There is an attempt taken in this dissertation to design and develop an embedded DC-DC converter suitable for high drop-out and embedded applications. However, the author targets for embedded applications (without external capacitor) and hence, one of the key objectives is to minimize the capacitors. In a conventional switch capacitor based converter, the output ripple decreases with the capacitor (flying capacitor and/or load capacitor) and increases with the load current. So the main constraints for low voltage low ripple on-chip DC-DC converters are high output ripple and low power efficiency due to the reduced value of on-chip implementable capacitance.

In the first proposed approach, along with a linear regulator a switched capacitor circuit is used to recycle charge for improving power efficiency. On the other hand the linear regulator helps to reduce the output ripple that is introduced by the switching circuit. Ripple reduction which is provided by the linear regulator is analyzed and optimized. The calculation of the power efficiency is done by the author. Here, the author proposes dual-switched capacitor circuits instead of using the fixed charge storing capacitor [30]. The second equal size flying capacitor is switching in opposite phase of that of the first one. This type of switched-capacitor configuration helps to reduce peak-peak ripple at the output of the switched capacitor circuit module. It also helps to maintain input supply current constant in contrast to rectangular profile with a single flying capacitor.

The output ripple is further reduced by introducing a synthesized ripple through the linear regulator. A detailed analysis and the necessary condition to minimize the output ripple are provided. Two switched capacitor circuits with appropriate phase difference are combined and fed to the linear regulator to provide a steady supply current to the linear regulator. Implementation of the proposed topology in the circuit level of design is described in detail in the dissertation. The performance of the dual switched capacitor based hybrid DC-DC converter is characterized in silicon by the author to prove the efficacy and limitation of the proposed topology.

It is observed by silicon characterization that the output voltage ripple of the dual switched capacitor based hybrid converter is still alarmingly high and power efficiency may be improved by using a new switching scheme. The output voltage ripple of on-chip dual switch-capacitor converter is improved by time-interleaving switching mechanism. Further improvement in output ripple and power efficiency is achieved by including a new switching scheme called Non-Overlapped Rotational Time-interleaving switching scheme (NRTI). This improvement is achieved by eliminating shoot-through current during switch-

ing transitions. As the stand alone switch-capacitor converter has poor line and load regulation, the NRTI switch-capacitor converter is integrated with a linear regulator through current regulation or voltage regulation control to improve its line and load regulations. The linear regulator actually helps to achieve the regulated output voltage at a pre-specified level. Moreover, the frequency and hybrid regulation are used for the improvement of power efficiency. The physical design of the NRTI DC-DC converter is also carried out. The NRTI switching scheme is also applied to generate $2Vdd/3$ and $Vdd/3$ output voltage level independently.

The last but not the least contribution in this dissertation is to develop a topology on dynamically reconfigurable step-down DC-DC converter. Here, the same flying capacitors are used to provide three different step-down fractions of its input supply and hence the power density of the converter is increased. In combination with a current control loop its output voltage can be adjusted dynamically over a wide range. It has also load sensing circuit which helps to dynamically reconfigure the switch capacitor module based on the instantaneous load requirement. This feature enables to extend the load current range to a higher limit and at the same time improves power efficiency in low load current regime.

So, in short, the author in this dissertation contributes to define a suitable topology of an embedded DC-DC converter (where load and flying capacitors are in on-chip implementable range) with improved power efficiency and very low output voltage ripple, suitable for low voltage applications.

The golden nuggets of the dissertation are as follows:

- Active ripple compensation of an embedded dual switched capacitor based hybrid DC-DC Converter and implementation on silicon to prove the efficacy of the proposed concept.
- To propose and implement a new switching mechanism, called non-overlapped rotational time interleaving scheme to eliminate the shoot through current loss and further reduction of the output voltage ripple.
- To propose and Design of a dynamically reconfigurable embedded NRTI Switched Capacitor based DC-DC Converter depending on the instantaneous load requirement.

Organization of the remaining part of the dissertation is as follows:

In chapter 2, the working principle and output ripple of a dual switched capacitor based hybrid voltage converter is described. The converter consists of a switching circuit module cascaded with a linear regulator. The switched capacitor circuit module is responsible for

stepping down the input supply voltage to half of its value with high power efficiency. However, this introduces a significant amount of output voltage ripple. This ripple is reduced by the linear regulator based on its power supply rejection ratio (PSRR). Apart from ripple reduction, the linear regulator is necessary to get line and load regulation of the converter. In addition, the dual switched capacitor based regulator is analyzed to predict two important performance metrics namely 'power efficiency' and 'output voltage ripple'. The expression for power efficiency of the converter is derived. Next, the small signal analysis and reduction of the ripple originated at the switched capacitor output by the linear regulator are presented. From the derived expression of supply-to-output ripple rejection, it is transparent that the attenuation offered by the linear regulator is high for the low frequency ripple. However, the amount of ripple at the output of the regulator is still alarmingly high for a high frequency ripple (say, beyond 50 MHz). This is because of the bandwidth limitation of the regulation loop in the linear regulator. Motivated by this urgency, a new technique for further reduction of high frequency ripple is introduced. A signal, synchronous to the original ripple (which comes from the switched capacitor module) is synthesized and it is fed into the linear regulator in such a way so that its effect at the output node counters the original ripple and hence, reduces the neat output ripple. The small signal analysis of the ripple synthesizer is carried out to formulate expression of the synthesized ripple current needed to cancel out the ripple originated from the switched capacitor converter. The improvement of ripple reduction has been substantiated by simulating the corresponding macro-model.

Chapter 3 is dedicated to the transistor level circuit design detail of the proposed dual switched capacitor based hybrid converter is described. Spice simulated results of the important circuit blocks are also provided. The two flying capacitors with each of 210 pF and the load capacitor is of 100 pF which can be implemented within the chip are used in the converter. Available 3.3 V thick gate oxide PMOS transistors with maximally permissible channel length is used to implement the flying and load capacitors. The maximum clock frequency of the internal clock generator employed is 35.6 MHz. and the converter can offer a regulated output voltage range of 1.26 V to 1.36 V for a load current range of 1.56 mA to 13.5 mA. Subsequent to the transistor level design, the physical design of the proposed dual switched capacitor based hybrid DC-DC converter is also presented. Description and importance of the placement of its different blocks is given here. Various notable issues and solutions related to the layout design of the test chip are also discussed.

Chapter 4 deals with the design of test board and brief description on different measurement setups. Different technical issues which are dealt during the design of the test board are elaborated here. It is also dedicated to the description of the measurement results and the corresponding analysis. Subsequently, simulated performance of the proposed converter system with different test options is compared with its measured performance. As expected,the simulated performance is the better one but the trends of measured results are matching with those of simulation results.
The measured power efficiency of the converter at 8.8 MHz of switching frequency and 12.7 mA of load current is 64.97%. However, the corresponding peak-peak output ripple as high as 604 mV. The ripple reduces to 146 mV at 35.6 MHz of switching frequency and the corresponding power efficiency degrades to 43.55%. Maximum power density 0.11267 $Watt/mm^2$ for total capacitor area of 0.15 mm^2. An extensive performance comparison is done with respect to the existing literature. From the comparative study it is seen that the measured power efficiency of the proposed converter system is 5.55% higher than the existing literature.

Chapter 5 discusses about a new switching scheme called Non-Overlapped Rotational Time-interleaving (NRTI) switching by which the output voltage ripple of a switched capacitor based converter is reduced. In addition to the ripple reduction, the proposed switching scheme also improves power efficiency. This improvement in power efficiency is achieved by eliminating shoot-through current during state transitions.
As the stand alone switched capacitor converter has poor line and load regulation, the NRTI switched capacitor converter is integrated with a regulation loop to improve its line and load regulation. Different type of regulation (such as, current control, frequency control, hybrid control and voltage control) schemes are discussed and implemented. The NRTI scheme is also applied to generate three different fractions of its input supply voltage viz., Vdd/2, 2Vdd/3 and Vdd/3.

In chapter 6 the NRTI switching based dynamically reconfigurable switched capacitor topology is proposed. In combination with the current control loop its output voltage can be adjusted dynamically over a wide range. It has a load sensing circuit which helps to dynamically reconfigure the switched capacitor module based on the instantaneous load requirement. This feature enables to extend the load current range to a higher limit and at the same time improves power efficiency in low load current regime. The hybrid control regulation scheme which is discussed in chapter 5 is also used here to improve the power

efficiency of the converter. This system is designed in a 0.18 μm CMOS technology for the conversion of 3.3 V (nominal) input voltage to a target output voltage ranging from 0.8 V-to-1.85 V.
Simulation results show that the peak power efficiency, maximum power density and the worst peak-to-peak ripple of the converter are 81.71$\%$ and more than 0.4 $Watt/mm^2$ and 20 mV respectively.

Finally the chapter 7 describes the insights and conclusions that are drawn from the dissertation. Also, the scopes for future work are presented.